Negative Differential Resistance and Instabilities in 2D Semiconductors
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LIGHT EMITTING LOGIC DEVICES BASED ON REAL SPACE TRANSFER IN COMPLEMENTARY InGaAs/InAlAs HETEROSTRUCTURES

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ABSTRACT

We discuss the principle and the implementation of novel light-emitting logic devices based on the real-space transfer (RST) of hot electrons between complementary conducting layers. One of these layers, the emitter, is doped n-type and has two or more contacts for applying the lateral electric field. Heated by this field, electrons are injected into a complementary p-type collector layer, contacted independently. The injection current is accompanied by a luminescence signal arising from the recombination of the transferred electrons in a specially designed collector active region.

The peculiar symmetry of charge injection by RST enables one to implement functional logic gates. The simplest structure with two emitter contacts acts as an exclusive OR gate in the dependence of both the collector current and the output light on the input voltages. The multiterminal device performs such functions as OR and NAND and is electrically reprogrammable between these functions. These powerful logic operations are demonstrated at room temperature.

We also review recent theoretical studies of the symmetry properties of RST transistors. These studies, based on continuation modeling and transient device simulation, reveal a variety of instabilities and a striking novelty of *multiply-connected* current-voltage characteristics. A RST transistor can support anomalous steady states in which hot-electron injection occurs in the absence of any voltage between the emitter electrodes. Some of these states break the reflection symmetry in the plane normal to the channel at midpoint. In the anomalous states, the electron heating is due to a fringing field from the collector electrode. The formation of hot-electron domains in real-space transfer represents a transition to such a collector-controlled state.

1. INTRODUCTION

An important direction in the microelectronics research is the development of new *functional devices*, which can perform logic tasks that would normally require an assembly of several transistors. The charge injection transistor (CHINT) offers interesting opportunities in this context.[1] The CHINT concept refers to a class of devices based on the principle[2,3] of real-space transfer (RST) of hot electrons between independently contacted conducting layers. Several functional devices employing this principle have been discussed in the literature.[4–8]

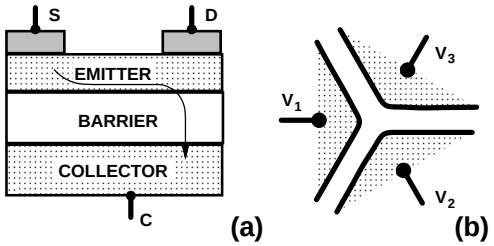
The generic CHINT structure is illustrated in Fig. 1a. One of the conducting layers, the emitter, plays the role of a hot-electron cathode, with the heating voltage applied to the contacts S and D. The other conducting layer, the collector, is separated by a heterostructure barrier. The RST effect manifests itself in the increase of the collector current I_C at a constant positive collector bias V_C, when a sufficiently high heating bias V_{DS} is applied.

A fundamental property of RST transistors, essential for our present discussion, is the *symmetry equivalence*[9,10] between the internal states $\mathcal{S}[V_D, V_C]$ of the device at different external bias configurations:

$$\mathcal{S}[V_D, V_C] \rightleftarrows \mathcal{S}[-V_D, (V_C - V_D)]\,. \qquad (1)$$

This correspondence follows from the reflection symmetry in the plane normal to the source-drain direction which cuts the channel in the middle. Although a similar relation exists between internal states $\mathcal{S}[V_D, V_G]$ in a field-effect transistor, there is an important difference in that the CHINT collector is the output terminal and the symmetry expressed by Eq. (1) implies that the output current is invariant under an interchange of the input voltages V_S and V_D. Thus the device exhibits an exclusive-OR (**xor**) dependence of the collector current on the input voltages, regarded as binary logic signals.

Even more powerful logic functionality is obtained in a RST device with three input terminals.[6] This device, which we shall refer to as the ORNAND gate, has a cyclic 3-fold symmetry, Fig. 1b. Its truth table (Fig. 1c) corresponds to $\mathbf{ornand}(\{\mathbf{V_j}\}) = \mathbf{or}(\mathbf{V}_1, \mathbf{V}_2)$ when $\mathbf{V}_3$ is low, and $\mathbf{ornand}(\{\mathbf{V_j}\}) = \mathbf{nand}(\mathbf{V}_1, \mathbf{V}_2)$ when $\mathbf{V}_3$ is high.



logic input	$\mathbf{V}_3$	0				1			
	$\mathbf{V}_2$	1	0	0	1	1	0	0	1
	$\mathbf{V}_1$	0	0	1	1	0	0	1	1
output	I_C	1	0	1	1	1	1	1	0
function		or				nand			

(c)

Fig. 1: Charge injection transistor principle and the RST logic.
(a) Schematic diagram of a CHINT. Emitter electrons, heated by the field applied between electrodes S and and D, undergo RST into the collector layer, as indicated by the arrow.
(b) ORNAND logic gate. Input terminals arranged with a 3-fold cyclic symmetry define three channels 1-2, 2-3, and 3-1.
(c) Truth table of $I_C(\mathbf{V}_1, \mathbf{V}_2, \mathbf{V}_3)$. The RST current is *off* in two states when $\mathbf{V}_1 = \mathbf{V}_2 = \mathbf{V}_3$ and *on* in the other six states. By symmetry, every *on* state has the same I_C.

The invention of charge injection logic[6] has focused attention on the symmetry properties of RST transistors. Their potential applications are likely to be based on the peculiar symmetry with respect to the heating field polarity. The same symmetry shows up in the analysis of the *instabilities* associated with the hot-electron injection and the domain formation in RST transistors. An unexpected recent discovery[9] is the existence of a number of anomalous states at $V_D = 0$, some of which are not only stationary but also *stable* with respect to small perturbations. In these states, the electron heating is due to the fringing field from the collector electrode. Because of the relation (1), states at $V_D = 0$ must either be symmetric with respect to reflections in the midplane normal to channel or possess broken-symmetry partners. By theoretical modeling of the CHINT operation it has been found[9] that the device possesses intrinsically complicated − often multiply-connected − IV characteristics. Application of a sufficiently high V_D at a fixed $V_C > 0$ forces a switching transition, accompanied by the formation of a hot electron domain. Physically, the domains form when the finite supply rate of electrons to a "hot spot" is exceeded by the RST flux from that spot. The depleted domains unscreen the fringing field ("normally" screened by channel electrons) and the RST becomes collector controlled.

Until recently, all of the work on CHINT and related logic devices involved heterostructures with the *same type of conductivity* in both the emitter channel and the collector. The review[10] cites a number of general references on unipolar real-space transfer transistors. Recently, one of us discussed[11] the possibility of using the RST of carriers into a *complementary* collector layer to implement light emitting devices endowed with a logic functionality with respect to electrical input. Significant progress in this program has been made in our laboratories during the last year. The first complementary CHINT was implemented in a InGaAs/InAlAs heterostructure and

demonstrated the **xor** operation.[12,13] Subsequently, the multiterminal ORNAND gate was implemented,[14] demonstrating the **or** and **nand** functions − both in the output light and the collector current − as well as the electrical switching between these functions.

The present work reviews the recent contributions.[12–14,9] The epitaxial structures used and the fabrication sequence are discussed in the next section. Electrical characterization of the complementary CHINT structures are described in Sect. 3, their optical characterization in Sect. 4, and the logic operation in Sect. 5. Results of the numerical simulation[9] of hot-electron transport in the simplest CHINT structure (Fig. 1a) are reviewed in Sect. 6. Our conclusions are summarized in Sect. 7.

2. STRUCTURES

Figures 2 show schematic cross-sections of the logic device structures discussed below. Structure of the XOR gate is illustrated in Fig. 2a and ORNAND gate in Fig. 2b. The $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ heterostructures have been grown by molecular beam epitaxy on InP substrate. The design is based on the epitaxial contact scheme, first used in the fabrication of CHINT by Mensz et al.[15] In this scheme, the channel length is defined by a trench etched in the n^+ cap layer (a), while the remaining portions of the cap layer make ohmic contacts to the source and drain metal. The 25 Å InAlAs layer (b) is used as an etch stop in the selective etching of the cap layer[16] All patterns, including the trenches, were defined by standard optical contact lithography.

In the ORNAND gate, instead of the triangular electrode arrangement of Fig. 1b, the required cyclic symmetry is obtained with four electrodes $1, 2, 3, \tilde{3}$ − two of which, 3 and $\tilde{3}$, being logically identical ($\mathbf{V}_{\tilde{3}} \equiv \mathbf{V}_3$) though physically split.

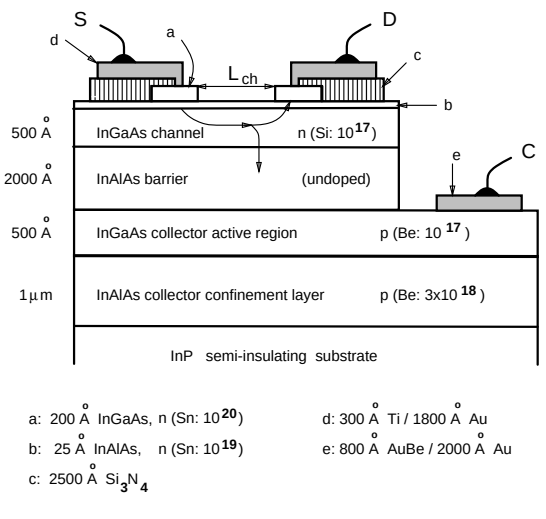


Fig. 2a: Cross section of the first complementary charge injection transistor.[12,13] The emitter channel length, defined by the trench etched in the cap layer (a), is $L_{CH} = 3\,\mu m$ and the width $W = 50\,\mu m$.

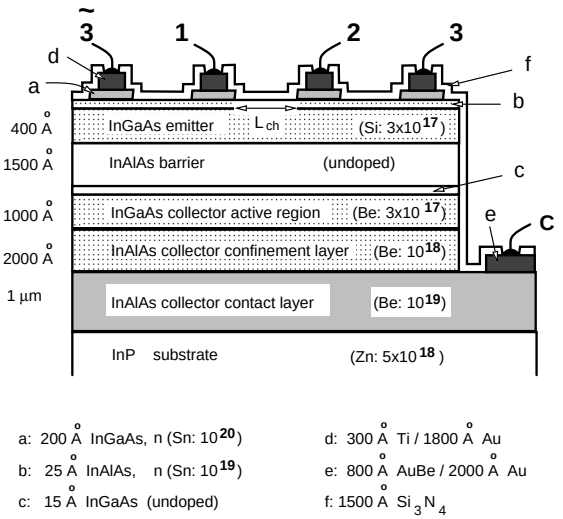


Fig. 2b: The ORNAND gate.[14] Each of the three channels, defined by trenches in the cap layer (a), has length $L_{CH} = 1\,\mu m$ and width $W = 40\,\mu m$. Cyclic symmetry results from the periodic boundary condition $\mathbf{V}_{\tilde{3}} \equiv \mathbf{V}_3$.

The epitaxial structures, shown in Figs. 2a and 2b are generally similar, but there are several noteworthy differences. The ORNAND structure is grown on a p-type substrate and uses a more heavily doped collector contact layer to reduce the parasitic series resistance in the collector circuit. The emitter channel is also more heavily doped to avoid its complete depletion by the surface potential and ensure a "normally-on" channel, which conducts even in the absence of a positive V_C.

Figure 3 shows a schematic energy-band diagram of the XOR device (Fig. 2a) in a cross-section under the trench. The corresponding diagrams for the ORNAND structure are quite similar, the main difference being that the emitter channel is not depleted ("normally-on") in equilibrium, due to heavier doping. In our XOR device in equilibrium, Fig. 3a, the channel is entirely depleted by the surface potential and the *pn* junction, so that the channel conduction requires a positive collector voltage to induce a two-dimensional electron gas at the interface with the barrier. In the "flat-band" condition, illustrated in Fig. 3b, the collector bias $V_C = V_{FB} \simeq 0.6\,\text{eV}$ corresponds to the work-function difference between *n*-InGaAs in the channel and *p*-InGaAs in the collector. In the operating regime, Fig. 3c, the *pn* junction is forward biased and the main obstacle to current is due to the band discontinuities at the two interfaces with the InAlAs barrier. Inasmuch as the valence band discontinuity in the InGaAs/InAlAs heterosystem is smaller than the conduction band discontinuity[17] ($\Delta E_V = 0.20\,\text{eV} < \Delta E_C = 0.50\,\text{eV}$) we can expect that, in the absence of RST, the collector current will be dominated by holes.

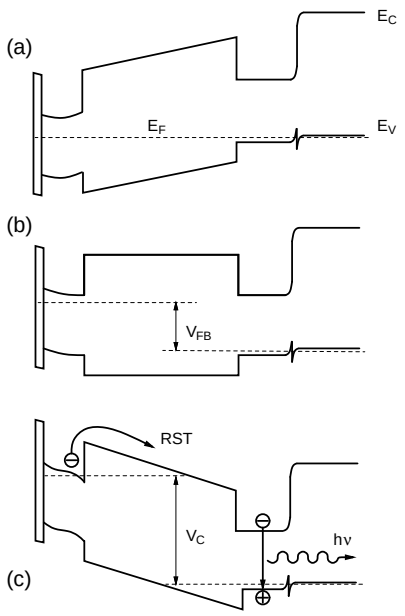


Fig. 3: Schematic energy-band diagram in a cross-section under the trench of the complementary CHINT of Fig. 2a.
(a) Equilibrium. The collector and the emitter-channel layers form a *pn* junction, separated by a wide-gap barrier. The channel is depleted by the surface potential.
(b) Flat-band condition. The flat-band voltage $V_C = V_{FB}$ is undetermined because of an uncertainty in the surface potential. The calculated flat-band voltage in a cross-section under the contacts is $V_{FB} = 0.63\,\text{V}$.
(c) Operating regime. The channel charge is induced by the collector field. When the heating electric field is applied along the channel, the latter becomes a hot-electron emitter. Real-space transferred electrons radiatively recombine with holes in the active region of the collector.

Electron heating is generated by a drain-to-source bias V_{DS}. The real-space transfer manifests itself in the increasing collector current I_C. As usual, it is accompanied by a negative differential resistance in the drain current I_D. In our complementary structures, the RST injection is accompanied by a $1.6\,\mu\text{m}$ luminescence signal, arising from the recombination of the injected electrons with holes in the InGaAs collector active region.

The purpose of the wide-gap InAlAs layer in the collector is to spatially confine electrons injected over the barrier and, at the same time, to provide a low-resistance path for the collector current. Both requirements are very important. Confinement is necessary for the radiative efficiency (otherwise most of the injected electrons would reach the collector contact prior to recombination) and low collector resistance is necessary to minimize a spurious back-gating effect, which would otherwise severely limit the available RST current. If the doping level N_A in the confining barrier is uniform, then a balance must be struck between the requirements of a low resistance (minimized by higher N_A) and a low recombination velocity at the interface between the active and confinement layers (minimized by lower N_A). A better solution, well-known in the art of designing heterostructure lasers, is to heavily dope most of the confinement layer but leave a thin low-doped sublayer immediately adjacent the active region. This approach was used (though by no means optimized) in the design of our more recent structure, Fig. 2b.

3. Electrical Characterization

Electrical properties of a complementary CHINT are quite different from those of unipolar devices.[4,10] Most of the differences are rooted in the fact that the collector and the emitter form a *pn* junction with a wide-gap barrier in between. The device operating regime corresponds to a forward bias of the *pn* junction, hence we must rely exclusively on the band-gap discontinuities to block the unwelcome leakage current. In what follows we shall refer to as the leakage that part of the collector current which flows independently of the electron temperature T_e controlled by the lateral field in the emitter channel. Identification of the leakage mechanism is an important part of the device characterization.

3.1 Leakage Current

In a unipolar RST transistor, the leakage can be strongly suppressed by choosing a heterostructure with a large conduction band discontinuity. Excellent results have been obtained[16] in the InGaAs/InAlAs system which has $\Delta E_C = 0.50\,\text{eV}$. In a complementary CHINT, we have to worry about the flux of holes from the collector into the emitter channel.

Figures 4 and 5a show the collector leakage current characteristics of the Fig. 2 devices with all emitter contacts grounded. The measured values of I_C are plotted against the collector bias V_C for different temperatures. At high temperatures, $T \gtrsim 200\,\text{K}$, and relatively low bias the current obeys the thermionic model

$$I_C = I_C^{SAT}\, e^{qV_C/n\,kT}\,, \tag{2a}$$

$$I_C^{SAT} = S\,A^*T^2\, e^{-\Phi/kT}\,, \tag{2b}$$

where n is the diode ideality factor, I_C^{SAT} the saturation current, S is the total emitter area including contacts, Φ is the barrier height at zero bias (separation between the hole Fermi level in the collector and the valence band edge in the barrier at the channel interface), and A^* the effective Richardson constant. From the slopes of the $I_C(V_C)$ curves at low bias, indicated by the dashed lines in Figs. 4 and 5a we determine $n \approx 1.4$. Extrapolating to $V_C = 0$, we determine I_C^{SAT} and find that it can indeed be fitted to the form (2b).

The inset to Fig. 4 and Fig. 5b show the Arrhenius plots of I_C^{SAT}/T^2 versus T^{-1} in the high-temperature range. The slopes of these plots give $\Phi = 0.90\,\text{eV}$ for the device in Fig. 2a and $\Phi = 0.84\,\text{eV}$ for the ORNAND device, Fig. 2b. These values are in reasonable agreement with calculated values Φ^h of the barrier height for holes relative to their Fermi level in the collector, based on the room-temperature energy gaps $E_G^{In_{0.53}Ga_{0.47}As} = 0.75\,\text{eV}$, $E_G^{In_{0.52}Al_{0.48}As} = 1.45\,\text{eV}$, the band discontinuities $\Delta E_C = 0.50\,\text{eV}$, $\Delta E_V = 0.20\,\text{eV}$, and given doping levels. The calculated values for the devices in Figs. 2a and 2b are, respectively, $\Phi^h = 0.89\,\text{eV}$ and $\Phi^h = 0.92\,\text{eV}$. This is to be contrasted with the estimated zero-bias barrier heights for emitter electrons, $\Phi^e = 1.10\,\text{eV}$ and $\Phi^e = 1.13\,\text{eV}$, respectively. The slight discrepancy between the measured and calculated values of Φ^h in the multiterminal device may be explained by a minor deviation of the actual doping levels from nominal or perhaps by thermally-assisted tunneling effects.

At higher collector biases, exceeding the flat-band condition $V_C > V_{FB}$, the top of the barrier for holes is at the collector interface. This is the operating regime of a complementary CHINT. Further increase of the collector current with V_C occurs primarily because of the accumulation of holes (increasing the Fermi level) and also, because of the increasing role of hole tunneling which lowers the effective barrier. Hence the leakage curve departs from Eq. (2) when $V_C > V_{FB}$. As is evident from Figs. 4 and 5a, in the operating regime the slope of $\log I_C(V_C)$ is relatively gentle. At low temperatures, $T \lesssim 150\,\text{K}$, thermally assisted tunneling of holes is the dominant leakage mechanism.

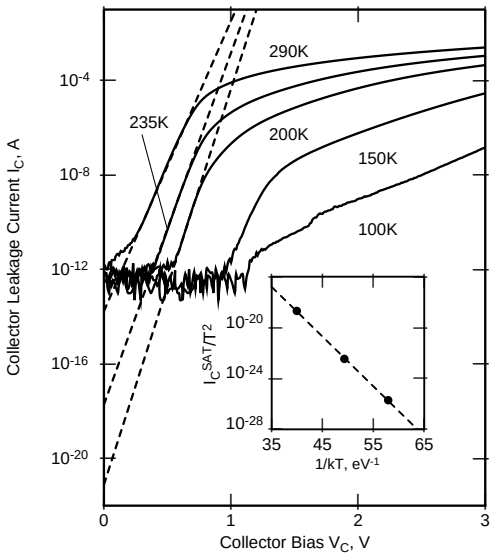


Fig. 4: Collector diode characteristics of the Fig. 2a device at different temperatures. Source and drain are connected together and grounded. Dashed lines indicate the linear extrapolation of I_C to zero forward bias. The intercepts of the dashed lines with the ordinate axis define I_C^{SAT}. Inset shows an Arrhenius plot of I_C^{SAT}/T^2. The measured activation energy $\Phi = 0.90\,\text{eV}$ agrees with $\Phi^h = 0.89\,\text{eV}$, calculated taking $E_F^e = 12\,\text{meV}$ and $E_F^h = 105\,\text{meV}$ for the equilibrium Fermi level separations from the conduction band in the emitter layer under the source/drain contacts and from the valence band in the collector active layer, respectively.

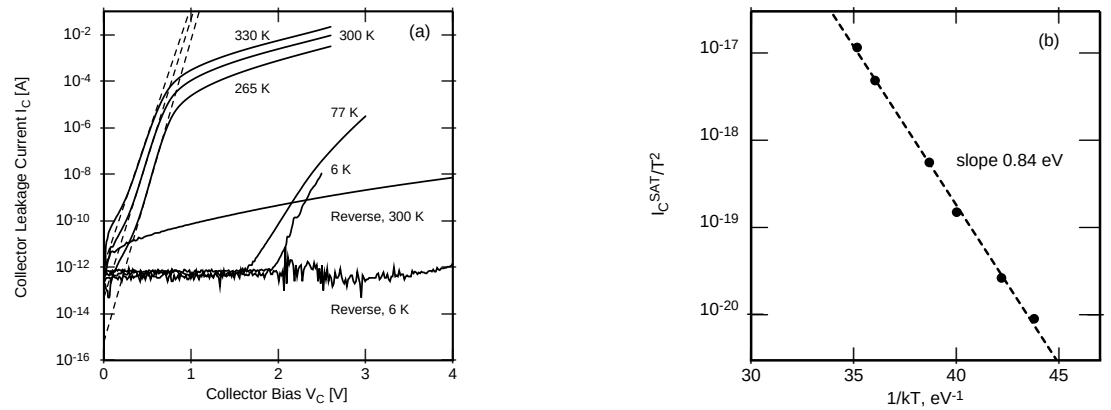
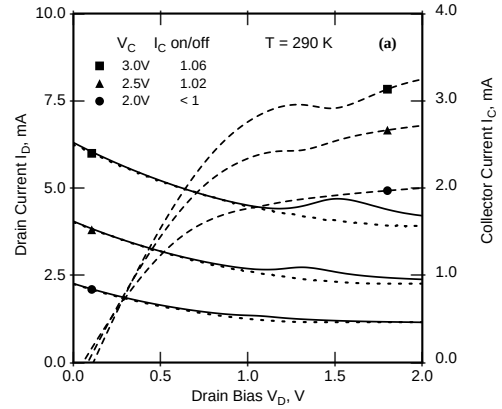
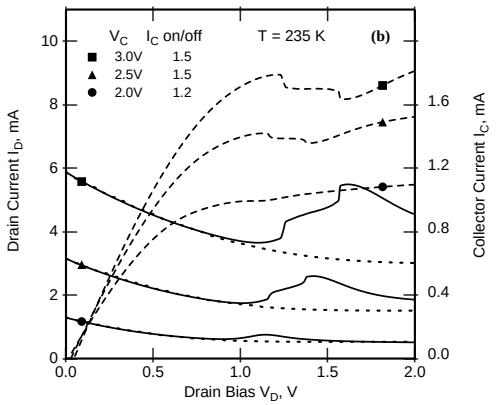


Fig. 5: Collector leakage current characteristics of the ORNAND device (Fig. 2b) at several temperatures. Curves $I_C(V_C)$ were measured with all four emitter electrodes grounded. Forward-biased collector-emitter *pn* junction corresponds to $V_C > 0$. The leakage current under reverse bias is of opposite polarity and the plotted curves represent $|I_C|$. Dashed lines in (a) indicate a linear extrapolation of $\log I_C$ to zero forward bias. From the Arrhenius plot (b) of the extrapolated value I_C^{SAT}/T^2 the activation energy is 0.84 eV. The calculated barrier height relative to the hole Fermi level is $\Phi_h = 0.92\,\text{eV}$, assuming $E_F^e = -21\,\text{meV}$ (degenerate) and $E_F^h = 82\,\text{meV}$ estimated from the given doping levels.

3.2 Transistor Characteristics

The usual way of presenting current-voltage characteristics of a charge injection transistor is to plot the family of $I_C(V_D)$ and $I_D(V_D)$ curves at constant values of V_C. Figures 6(a)-(c) show such characteristics of the complementary CHINT at $T = 290\,\text{K}$, $T = 235\,\text{K}$, and $T = 100\,\text{K}$. The low V_D part of the characteristics is similar to that in a "normally-off" field-effect transistor (FET), with the collector playing the role of a gate. At a fixed V_C and increasing the heating voltage V_D, the channel current first ($V_D \lesssim 0.5\,\text{V}$) increases linearly, then sublinearly with a tendency for saturation. The saturation value of the current increases with V_C, as it would in a FET. When the heating voltage is high enough to establish a significant RST, the drain current shows a negative differential resistance (NDR). The NDR effect is enhanced at lower temperatures, where it manifests itself by an abrupt drop in I_D. Simultaneously, the collector current rapidly increases from its leakage value.





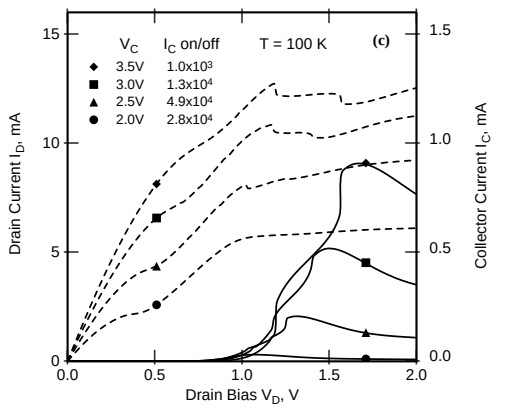


Fig. 6: Current-voltage characteristics at different temperatures and collector biases V_C. Drain current I_D is shown by the dashed lines and collector current I_C by the solid lines. The dotted lines show the expected leakage behavior of I_C in the absence of RST, calculated from Fig. 4. The collector current on/off ratio is calculated by dividing the (relative) maximum value of I_C by its minimum value before the onset of real-space transfer.
(a) $T = 290\,\mathrm{K}$; (b) $T = 235\,\mathrm{K}$; (c) $T = 100\,\mathrm{K}$.

Note that the increase in I_C does not fully compensate for diminishing I_D, which means, by Kirchhoff's law, that the source current also decreases. This behavior can be explained by two mechanisms, both due to the backgating effect of the collector field. The first mechanism, which might be termed intrinsic, is due to the charge dynamically stored in the barrier layer in transit toward the collector.[4] The negative dynamic charge partially screens the collector field and reduces the electron concentration in the emitter channel. The second mechanism is due to a negative feedback of the collector current in the presence of a parasitic series resistance in the collector path. When the RST current begins to flow, the voltage drop on that series resistance reduces the collector potential, effectively lowering the V_C. Both effects result in decreasing the source current. When the collector contact is not properly alloyed, the series resistance may dominate.† In our device the dynamic space-charge effect may account for most of the decrease in the source current, as can be ascertained by simple estimates.[4] Nevertheless, a residual collector series resistance ($R_C \lesssim 0.5\,\mathrm{k\Omega}$ at $290\,\mathrm{K}$ but higher at lower temperatures, see below) is likely to be present in our structure; without R_C we find it hard to understand certain features in the characteristics at high V_D and still higher V_C.

Indeed, as seen from Figs. 6, the collector current shows a well-defined maximum as a function of V_D. This behavior is faithfully tracked by the electroluminescence signal, which, as discussed in Sect. 4, indicates that the maximum is associated with a decrease of the electron RST current at high V_D. We believe, that the existence of a peak in the collector current and the decrease of I_C at higher V_D is related to the increase in the potential of the "hot spot" (i.e. the high-field region in the channel where

† Such structures usually show a giant NDR accompanying a relatively little RST current. This anomaly goes away upon annealing the alloyed contact.

most of the RST occurs) relative to the collector. Reversal of the field in the barrier at the hot spot exponentially suppresses the RST. No peak in I_C is observed when V_D is increased *simultaneously* with increasing the collector voltage, which corresponds to varying the source voltage at fixed V_D and V_C. Field reversal at the hot spot naturally explains our data in Fig. 6 at lower $V_C \leq 2.5\,\mathrm{V}$. However, a close examination of Fig. 6c shows that it does not work directly for higher values of V_C. Thus, for $V_C = 3.5\,V$, the maximum occurs near $V_D = 1.7\,\mathrm{V}$. In the absence of a collector resistance, this would suggest that the entire emitter channel is in the operating regime and no field reversal takes place at the hot spot. To make the ends meet, it is sufficient to assume a series resistance $R_C \approx 1\,\mathrm{k\Omega}$ in the collector circuit at low temperatures.

Consideration of the parasitic series resistances is also necessary to disentangle the RST from cold carrier leakage, which is important for estimating the internal radiative efficiency, especially at higher temperatures (see Sect. 4). In the higher-temperature plots, Fig. 6a and 6b, the collector current is seen to decrease prior to the onset of the RST. This is due to the diminishing leakage current with decreasing collector-to-drain bias. The same behavior occurs at low temperatures, but on the scale of Fig. 6c the leakage is not resolved. In order to estimate the RST current at higher temperatures, it is necessary to subtract the leakage contribution from the measured collector current. Ideally, when the junction in the drain region is near flat bands, the leakage from that region is effectively shut off and the overall leakage must diminish roughly by a factor of 2. However, as discussed below, inclusion of the parasitic resistances somewhat complicates the analysis.

We would like to distinguish between two contributions to the collector current:

$$I_C = I_C^{\mathrm{LKG}} + I_C^{\mathrm{RST}}\ , \tag{3}$$

where I_C^{RST} is the real-space transfer current of hot electrons and I_C^{LKG} is the collector leakage, defined as the current which would flow at a given voltage configuration (V_C, V_D) if the electron heating phenomenon were absent. Both I_C^{LKG} and I_C^{RST} depend on the voltages V_C and V_D. To estimate the behavior of the leakage component, we use an approximate equivalent circuit, shown in Fig. 7a. The FET symbol represents the "intrinsic" portion of the device under the trench; contribution of this area to the leakage current is assumed negligible. The diode symbols correspond to the *pn* junctions in the source and drain contact areas (it should be noted here that our "diode" is not a conventional *pn* junction, but has a heterostructure barrier separating the *p* and the *n* regions). For the purpose of calculating the leakage, we neglect the RST. The resistors R_S, R_D, and R_C represent parasitic series resistances in the source, drain, and collector, respectively.

It would be nice to be able to determine the equivalent circuit parameters by a least square fit, but our data are insufficient for that purpose. Figure 7b illustrates the situation. The solid line represents the $I_C(V_D)$ curve at $V_C = 2.5\,\mathrm{V}$ and $T = 235\,\mathrm{K}$. We are interested in establishing the leakage component near the peak of the RST current at $V_D \approx 1.4\,\mathrm{V}$ by extrapolating the pre-RST behavior corresponding to $V_D \lesssim 1\,\mathrm{V}$. We use the circuit of Fig. 7a, assuming a perfect symmetry between the source and the drain and taking the single diode characteristic from the data of Fig. 4a. Dashed curve (a) corresponds to letting all the series resistances vanish. Adding a collector resistance shifts the curve upwards (b). A source resistance shifts it downwards (d,c) − in large part because of the voltage drop associated with the source-to-drain current. A good fit can be achieved with a continuous range of combinations of assumed R_S and R_C, which means that the values of these resistances cannot be determined in this way. The use of our procedure derives from the fact that the asymptotic value of the leakage is insensitive to the actual values of R_S and R_C, so long as they give a good fit to the region $V_D \lesssim 1\,\mathrm{V}$. If we tried to use a simple spline fitting instead, we would need to specify a value for the horizontal asymptote − which cannot be determined lacking a physical basis.

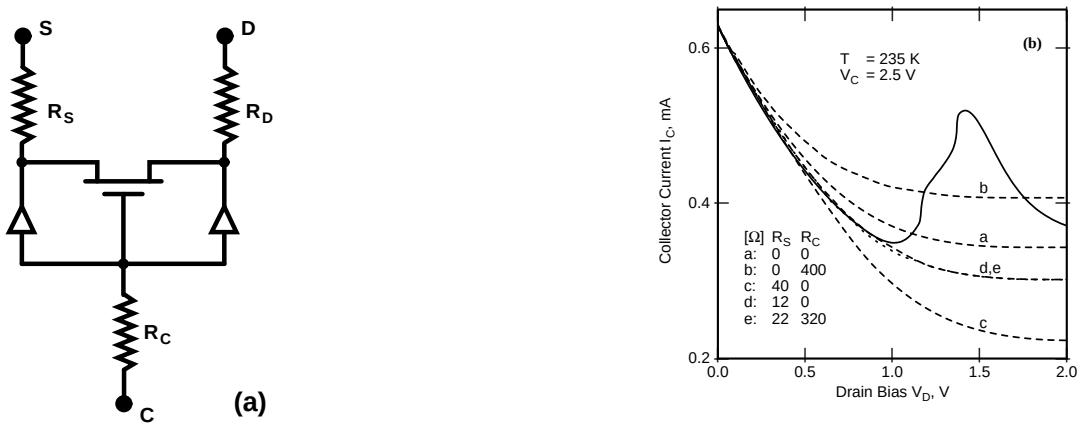


Fig. 7: Illustration of the procedure for estimation of the leakage current.
(a) Circuit model. The FET symbol represents the emitter channel assuming no RST current. The diodes correspond to *pn* heterostructure under the source and drain contacts and the resistors R_S, R_D, and R_C to parasitic series resistances in the source, drain, and collector current paths, respectively.
(b) Estimation of the leakage current at a particular temperature and V_C. Characteristic of the FET symbol (the channel current) is taken from Fig. 6b. Diode characteristics are taken from Fig. 4. Series resistances are assumed symmetric, $R_D = R_S$.

The leakage curves, $I_C^{LKG}(V_D)$, determined in the indicated fashion for each value of V_C, are plotted by the dotted lines in Figs. 6a and 6b. Subtracting the leakage curve, we obtain a reasonable approximation to the RST current I_C^{RST} at a given bias. Thus calculated curves $I_C^{RST}(V_D)$ are used below in Sect. 4.

3.3 Characteristics of a Single ORNAND Channel

The multi-terminal logic device actually forms three channels: $1-2$, $2-3$, and $\tilde{3}-1$. In the description of this device we shall use an arrow to indicate the source$\rightarrow$drain direction in a particular measurement. Figure 8 shows the typical room-temperature characteristics, measured in the channel $\tilde{3}\rightarrow 1$. Characteristics of different channels coincide quite closely, but there is a slight asymmetry under the source-drain interchange in a single channel, due to an unavoidable off-center misalignment of the trenches. Thus the $\tilde{3}\rightarrow 1$ characteristics are slightly different from those measured in the $1\rightarrow\tilde{3}$ configuration. As shown in Sect. 5, this systematic asymmetry cancels out in all the 8 states of the ORNAND gate.

Single-channel characteristics of the multiterminal device are significantly improved over those in Fig. 6a for the three-terminal CHINT of Fig. 2a. The key improvement lies in the larger I_C^{RST}, which is moreover achieved at lower V_C. This improvement can be attributed to a reduction of parasitic resistances. The present device, because of its multiterminal nature, naturally lends itself to a measurement of the series resistance R in electrodes 1 and 2. We have found $R = (10 \pm 1)\,\Omega$, dominated by the contact resistance. The outer electrodes can be expected to have slightly lower R.

The I_C^{LKG} contribution, calculated using the diode characteristics of Fig. 4a, is plotted in Fig. 8 by the bold dotted line. No parasitic resistance was assumed in this case, but we included the asymmetry in the emitter area associated with the source (electrode $\tilde{3}$) and the drain (electrode 1) when the other two contacts are floating.

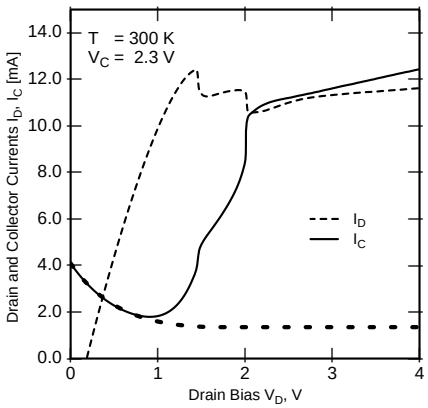


Fig. 8: Room temperature current-voltage [$I_C(V_D)$ and $I_D(V_D)$] characteristics of a single-channel $\tilde{3}\rightarrow 1$ at a fixed collector bias $V_C = 2.3\,\mathrm{V}$. Electrode $\tilde{3}$ is grounded and 1 acts as the drain. Electrodes 2 and 3 are kept floating. The bold dotted line indicates the leakage component I_C^{LKG}, calculated from the data in Fig. 5a.

Note the absence of a peak in the collector characteristic of Fig. 8, to be contrasted with the data in Fig. 6. At this point, we attribute this difference to a heavier channel doping in the multiterminal structure; a conclusive analysis requires an accurate two-dimensional simulation of the complementary device that we have not yet carried out.

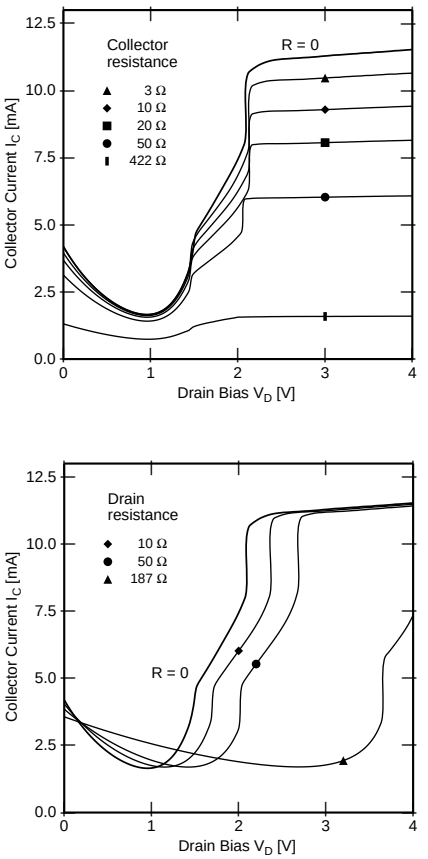


Fig. 9: The effect of series resistances. Current voltage characteristics $I_C(V_D)$ of a single channel $\tilde{3}\rightarrow 1$ measured under the same conditions as in Fig. 8 (though in a different device) with series resistances R added in (*a*) the collector, (*b*) the source, and (*c*) the drain circuits.

The effect of adding external series resistances is illustrated in Fig. 9. Resistors in series with the source or the collector have a similar effect: its voltage drop effectively reduces the collector-to-source bias. The latter affects the normal electric field in the barrier and the sheet carrier concentration in the channel. A drain series resistance, on the other hand, reduces only the lateral channel field with the effect that the same I_C is reached at a higher V_D.

Figure 10 reports a new and interesting finding. It shows the current-voltage characteristics for a grounded collector, both at $300\,\mathrm{K}$ and $6\,\mathrm{K}$. The built-in electric field at $V_C = 0$ opposes the RST of channel electrons and increases the effective barrier

height, cf. Fig. 3a. For $V_D > 0$, the device cross-section near the drain is a reverse-biased *pn* heterojunction. One would expect the characteristics to be similar to those in Fig. 5a for the reverse collector biases $V_C < 0$. However, at a certain drain bias, the curves $I_C(V_D)$ in Fig. 10 depart from the reverse-bias leakage curves, with the current increasing by several orders of magnitude. Such a regime has not been observed in the structure of Fig. 2a, where the emitter doping is lower and the channel is "normally off", so that the transport properties at $V_C = 0$ can not be properly investigated. Channel characteristics of the ORNAND structure closely resemble those in a normally-on field-effect transistor and show no particular structure in the anomalous region.

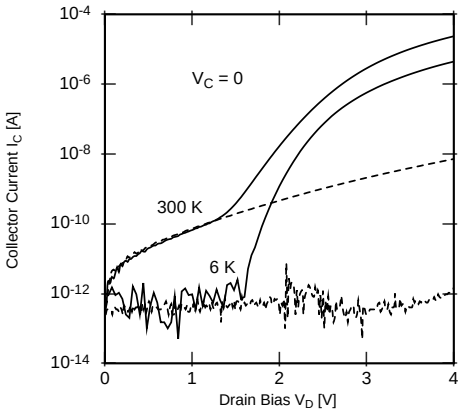


Fig. 10: Anomalous current-voltage characteristics of a single channel $\tilde{3} \rightarrow 1$ at $V_C = 0$ and two different temperatures. Electrodes 2 and 3 are floating. Solid lines show $I_C(V_D)$ at $V_C = 0$. Polarity of I_C corresponds to the flow of holes from the channel into the collector. Dashed lines represent the reverse-bias collector leakage current from Fig. 5a. The "soft breakdown" near $V_D \simeq 1.5\,V$ is attributed to the RST of impact-ionized holes.

We believe the sharp rise of the reverse collector current (polarity corresponding to electrons flowing from the collector into the channel) at high values of $V_D \gtrsim 1.5\,\mathrm{V}$ can be imputed to the *impact ionization* by hot electrons in the channel. Holes, released by this process near the drain, drift toward the source and undergo a substantial heating along the way. The observed increase of $|I_C|$ is thus interpreted as a RST of *minority holes* from the channel. Note that the same electric field that suppresses the RST of electrons aids the RST of channel holes. Injection of *majority* carriers into the collector does not give rise to a luminescence − which is in accordance with our experimental observations. At cryogenic temperatures, the ionization threshold in InGaAs increases due to the band-gap widening and so does the critical value of V_D at which the $I_C(V_D)$ curves in Fig. 10 depart from the corresponding leakage curves. Evidently, the complementary structure is not essential, although it simplifies observation of the minority RST effect by reducing the leakage current under reverse bias. The RST of minority carriers can be a powerful tool for studying impact ionization phenomena in field-effect transistor channels.

4. OPTICAL CHARACTERIZATION

Electroluminescence of the complementary RST devices was detected from the back of the polished substrate using a liquid nitrogen cooled Ge detector and a 0.75 m spectrometer. We observed a spectrum peaked at the photon energy corresponding to the band-to-band recombination in InGaAs. As the bandgap shrinks with increasing temperature, the peak wavelength increases from $1.56\,\mu\mathrm{m}$ at $T = 100\,\mathrm{K}$ to $1.59\,\mu\mathrm{m}$ and $1.60\,\mu\mathrm{m}$ at 235 K and 290 K, respectively. Moreover, at low temperatures ($\lesssim 100\,\mathrm{K}$) the position of the peak slightly shifts towards higher energy as the RST current increases. We attribute this shift to a band-filling effect due to the increasing electron injection. To measure the total emitted power, we used a broad-area Ge photodiode and suitable focusing optics.

Figures 11 show the dependence of the measured light power P_L on the electron heating voltage V_D at selected temperatures and different values of V_C. On the same graphs we show the "net" RST curves $I_C^{RST}(V_D)$, calculated as described in Sect. 3.2. The first notable observation is that the $P_L(V_D)$ curves are to a good degree proportional to

$I_C^{RST}(V_D)$, rather than to the total $I_C(V_D)$ of Fig. 6, as one could naively expect. Accordingly, the measured optical on/off ratio (Figs. 11) far exceeds the on/off ratio in the collector current, the difference being particularly striking at low temperatures. Even at $T = 290\,\mathrm{K}$, where the RST structure in $I_C(V_D)$ is barely visible against the leakage background, the corresponding modulation of the optical signal is by an order of magnitude: for $V_C = 3.0\,\mathrm{V}$ the on/off ratio is 9 in P_L and 1.1 in I_C. The origin of this remarkable performance must be clearly understood, since the depth of modulation is of paramount importance for room-temperature logic applications of the light-emitting RST devices.

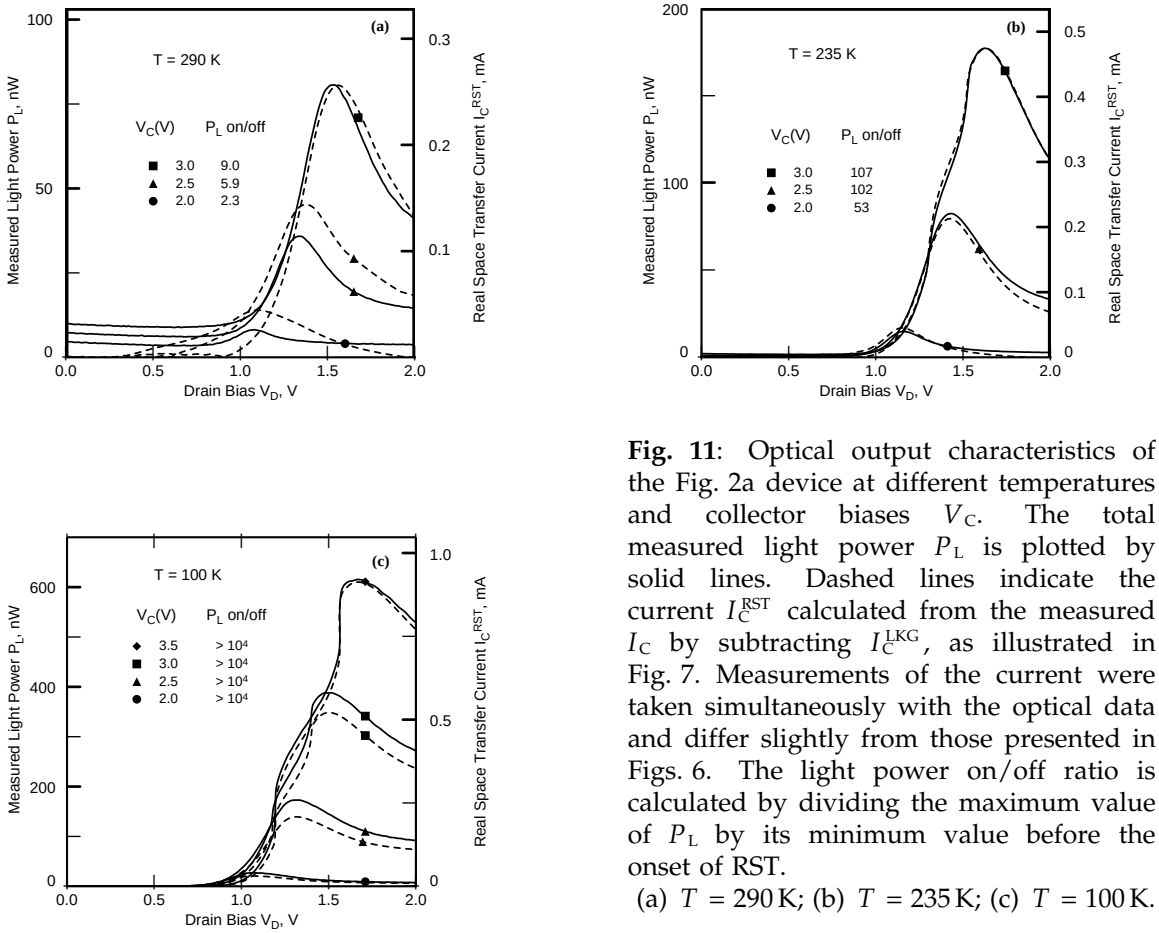


Fig. 11: Optical output characteristics of the Fig. 2a device at different temperatures and collector biases V_C. The total measured light power P_L is plotted by solid lines. Dashed lines indicate the current I_C^{RST} calculated from the measured I_C by subtracting I_C^{LKG}, as illustrated in Fig. 7. Measurements of the current were taken simultaneously with the optical data and differ slightly from those presented in Figs. 6. The light power on/off ratio is calculated by dividing the maximum value of P_L by its minimum value before the onset of RST.
(a) $T = 290\,\mathrm{K}$; (b) $T = 235\,\mathrm{K}$; (c) $T = 100\,\mathrm{K}$.

By studying the temperature dependence of $I_C(V_C)$ at $V_D = 0$, we had concluded in Sect. 3.1 that the collector leakage is mostly due to the injection of holes into the channel. Now, the data of Fig. 11 clearly indicate that this injection does not contribute to the optical signal. It is significant that the leakage and the RST are caused by different types of carriers. The injected holes have a vastly lower radiative efficiency because they are likely to reach the source or drain contact before they recombine radiatively with electrons. The $In_{0.52}Al_{0.48}As$ etch-stop layer *b* (Fig. 2) is insufficiently thick to confine minority holes in the emitter channel (the estimated hole escape time by tunneling across this layer is much shorter than the radiative recombination time). Most of the nonradiative recombination is likely to occur in the layers heavily doped with tin. In contrast, electrons injected into the collector are confined in the active region. Virtually all of the optical output can be attributed to the recombination of injected electrons in the collector active layer. This implies an important design consideration: to maximize the optical on/off ratio it is essential to suppress the leakage of electrons into the active region; the oppositely directed flux of holes can be tolerated.

At low temperatures, Fig. 11c, the light signal related to the leakage is below the noise level and the on/off ratio in P_L is above 10^4. At higher temperatures, the small electron component of the leakage current increases and consequently the on/off ratio disparity between the light-power output and the collector current is less pronounced. From the measured light power $P_L(V_D, V_C)$ we can estimate the internal radiative efficiency of the RST electrons as follows:

$$\eta_q = \frac{1}{h\nu\,\eta_c\,t_o}\,\frac{q\,\Delta P_L}{I_C^{RST}}\,, \tag{4}$$

where $\eta_c \approx 0.48\,\%$ is the collection efficiency (estimated assuming an isotropic emission over the 2π solid angle, due to reflection from the surface metallization), $t_o \approx 88\,\%$ is the combined transmission of the optical components (lens and windows) between the detector and the device, and $h\nu$ is the photon energy at the peak of the luminescence spectrum. To account for the light power due to the leakage current, the quantity ΔP_L is taken equal to $P_L(V_D, V_C)$ minus the optical power measured at the same V_C but lower V_D, prior to the onset of the RST. At lower temperatures, one has $\Delta P_L = P_L$.

The fact that our collection efficiency η_c is low, is accounted for by the total internal reflection, Fresnel loss, and the collection solid angle. We have not used an anti-reflection coating. The relatively low numerical aperture ($N_A \approx 0.34$) has been forced by the use of a dewar for low-temperature measurements. Moreover, an error of $\pm 5\,\%$ in N_A from the collection lens being slightly out of focus, produces an error of $\pm 10\,\%$ in η_c. Nevertheless, the systematic error in the determination of the efficiency was the same for all measurements, since the lens system was not adjusted during the whole set of measurements. The *relative* efficiency behavior at different temperatures and biases can be considered quite reliable.

Figure 12 shows the basic trends in the behavior of the radiative efficiency η_q under varying temperature and collector bias. We found that near and above the peak of the RST current the efficiency is not modulated by varying V_D. This means that η_q is practically independent of the injection current at a given T and V_C. The data in Fig. 12 is taken near the RST peak; the dependence on V_D in a wider range is discussed below. As is evident from the figure, the radiative efficiency decreases with increasing temperature. This dependence is likely to be explained, as in conventional light-emitting devices, by the increasing role at higher T of non-radiative processes, such as Auger recombination.[18]

It is instructive to consider the radiative efficiency of the leakage current itself. This can be characterized by a parameter η_q^{LKG}, defined as in Eq. (4) but with ΔP_L replaced by $P_L(V_D=0)$ and I_C^{RST} by the total I_C at zero heating bias. For $V_C = 3.0\,V$ and $T = 290\,K$, $235\,K$, and $200\,K$, we find $\eta_q^{LKG} = 0.12\,\%$, $0.06\,\%$, and $0.04\,\%$, respectively. This temperature dependence, "opposite" to that in Fig. 12, gives a further evidence to the fact that the leakage light is due not to a small fraction of holes that recombine radiatively in the emitter channel but to a small electron contribution to the leakage current.

Returning to Fig. 12, the efficiency is also seen to decrease with increasing collector bias. This effect is prominent only at low $T \lesssim 150\,K$ (no significant variation of η_q with V_C is observed at higher temperatures; the apparent dependence at $T \gtrsim 200\,K$ in Fig. 12 is not meaningful since the low-V_C points are within an experimental error introduced by the uncertainty in the subtraction of the leakage component). One possible explanation for the V_C dependence may be related to the injection of hot electrons into the wide-gap collector confinement layer, where they recombine nonradiatively.† Within this model, weakening of the V_C dependence of η_q at higher

† Even if there were a radiative component from the confinement layer, it would not be detected experimentally, since all of the InAlAs light output would be re-absorbed in the InP substate. Moreover, as a matter of principle, one would not expect a significant radiation from the wide-gap layer, since electrons there are no longer confined and their radiative lifetime is longer than travel

temperatures can be explained by a shorter hot-electron mean-free path due to higher rate of optical-phonon scattering. The fact that a sizable fraction of injected electrons can retain enough energy (especially at lower temperatures) to clear the second barrier, is well known from studies of ballistic transistors (see, for example, Ref. 19 and the literature cited therein). This interpretation does not contradict the fact that our measured spectra do not show hot-electron tails, because the electron cooling rates in InGaAs are known[20] to be faster than recombination.

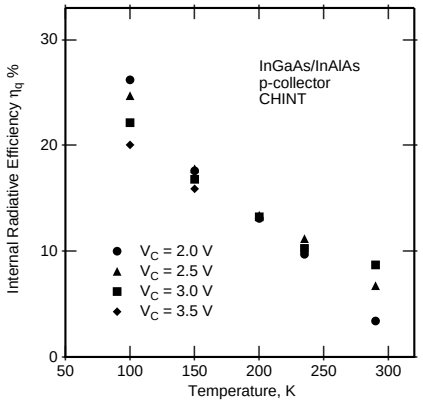


Fig. 12: Dependence of the internal radiative efficiency η_q on the lattice temperature for different collector biases.

Nevertheless, we have difficulties with this interpretation. First, it is inconsistent with our understanding of the peak in the $I_C(V_D)$ dependence, which we had attributed in Sect. 3.2 to a field reversal in the "hot-spot" region of the channel. Clearly, one would expect a suppression of the ballistic-transistor effect in this case. This contradicts our data in Fig. 13a, which shows the dependence of the calculated η_q on the heating voltage V_D for several values of V_C at $T = 100\,\mathrm{K}$. No enhancement of the η_q occurs at the heating voltages V_D above the I_C peak.

Next, consider the most striking feature of Fig. 13a, namely the dramatic downward steps in the efficiency, accompanying steps in the collector current. The low-bias values of the efficiency are relatively high and largely *independent* of the collector voltage.† As the heating bias reaches the location of the first current step, the efficiency suddenly drops to a lower plateau value. Moreover, curves corresponding to lower collector biases ($V_C = 2.0$ and $2.5\,\mathrm{V}$), at which there are no steps in the current-voltage characteristics, show no significant decrease in efficiency either. For $V_C > 2.5\,\mathrm{V}$, something evidently happens near $V_D \approx 1.2\,\mathrm{V}$ which forces the step-like switching of the current and is accompanied with the efficiency drop. Steps in the current-voltage characteristics of the CHINT are usually explained[4,9,10,15,21,22] by an instability associated with the formation of hot-electron domains in the channel. Both the field and the electron temperature T_e rise dramatically in the domains and that, of course, may lead to a higher injection into the confinement layer, because of the higher average energy of injected electrons. However, if the injection energy is the deciding factor, then we should expect the radiative efficiency go down strongly with increasing V_C at all values of V_D. The trouble with the above ballistic-transistor interpretation of the $\eta_q(V_C)$ dependence is not that we cannot stretch it to explain the efficiency drop (*that* we can

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time to the contact.

† The apparent decrease in η_q at lowest heating biases (near the sensitivity limit of our light detector) is probably related to nonradiative recombination with defects. The rate of such processes scales linearly with the minority concentration and at low carrier injection it exceeds the radiative recombination rate.

do!) but that it is clearly inconsistent with the fact that low-V_D values of η_q are practically *independent* of V_C. We are, therefore, led to consider alternative interpretations of the efficiency data.

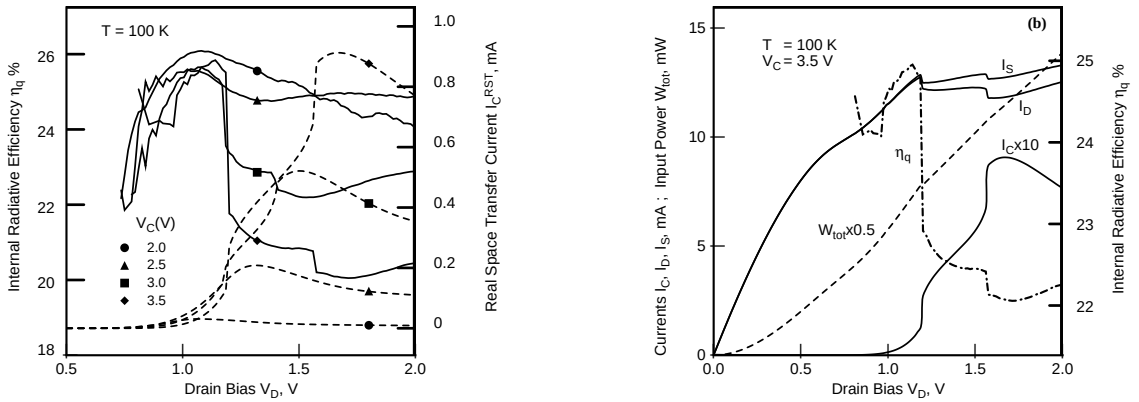

Fig. 13: Dependence of the internal radiative efficiency η_q on the heating voltage V_D.
(a) Plots at different collector biases. Dashed lines indicate I_C from Fig. 6c.
(b) Simultaneous plots of the radiative efficiency (η_q), the drain, collector, and source currents (I_D, I_C, and I_S, respectively), and the total electrical input power (W_{tot}).

In our opinion, a possible explanation involves a nonlocal heating of the lattice by hot electrons. In this picture, the lattice temperature in the active layer may substantially deviate from the ambient temperature, due to the power W_e dissipated by hot-electrons in the channel via optical-phonon emission. This power can be estimated as

$$W_e = \mathcal{A}\,\frac{n\,kT_e}{\tau_e}\,, \tag{5}$$

where n is the sheet carrier concentration in the emitter channel at the hot spot, $\mathcal{A}$ the hot-spot area, and $\tau_e(T_e)$ the energy relaxation time of hot electrons at temperature T_e. At low V_D the heating field in the channel is low and relatively uniform, hence T_e is low and so is W_e. The formation of a hot-electron domain shrinks $\mathcal{A}$ but at the same time strongly increases T_e and therefore W_e goes up. Higher phonon emission in the channel leads to a higher lattice temperature in the collector active layer and hence a lower radiative efficiency. From the data of Fig. 12, the required temperature increase at $T = 100\,\mathrm{K}$ is by less than $50\,\mathrm{K}$. The dependence on V_C results from the field-effect gating action of the collector, expressed in Eq. (5) by the factor $n(V_C)$. After the domain is formed, the dependence on V_D is weak.

We would like to stress that the lattice heating by hot carriers is an essential part of this picture. A simple Joule heating of the whole device is ruled out by the following observation. Consider the total input power W_{tot} into the transistor, which in the common-source configuration is given by

$$W_{tot} = I_C V_C + I_D V_D\,. \tag{6}$$

To our surprise, we found that W_{tot} is *continuous* at the steps in the current-voltage characteristics.§ This is illustrated in Fig. 13b, which shows the behavior of one of the

§ In addition to our present device, we have re-analyzed the available data measured in previously reported unipolar charge injection transistors. To our surprise, we found that most (but not all) steps in I_D, I_C, and $I_S = I_D + I_C$ are accompanied by a continuous variation in the total input power. Typically, only the slope $W_{tot}(V_D)$ changes at the transition. We believe this phenomenon deserves further study, both experimental and theoretical. It may shed light on the nature of switching transitions between different branches of intrinsically complicated trajectories[23] in the device phase

efficiency curves of Fig. 13a together with I_D, I_C, I_S, and W_{tot}. We see that while all the terminal currents experience a discontinuity at $V_D \approx 1.2\,V$, the total power input remains continuous.

To avoid misunderstanding, let us remark that W_e is only a part of W_{tot}. Most of W_{tot}, however, is dissipated by acoustic phonons and distributed over a large volume. In contrast, the power W_e, dissipated by electrons with $T_e > \sim 1\,000\,K$, goes into the generation of relatively immobile optical phonons at the hot spot.

We conclude this Section by displaying in Fig. 14 the room-temperature light-voltage characteristics of a single-channel $(\tilde{3} \to 1)$ of the multiterminal device. These characteristics were taken under the bias conditions identical to those in Fig. 8. For comparison, the figure also shows the I_C^{RST} curve, obtained by subtracting I_C^{LKG} (shown in Fig. 8 by the bold dotted line). We see that even though the injection current increases monotonically, the P_L curve has a maximum − like the analogous curves in Fig. 11 − although the drop after the maximum is not so steep. At this time, we do not have a clear understanding why the two curves shown in Fig. 14 have a different behavior at $V \gtrsim 2\,V$, cf. our comment below Fig. 8.

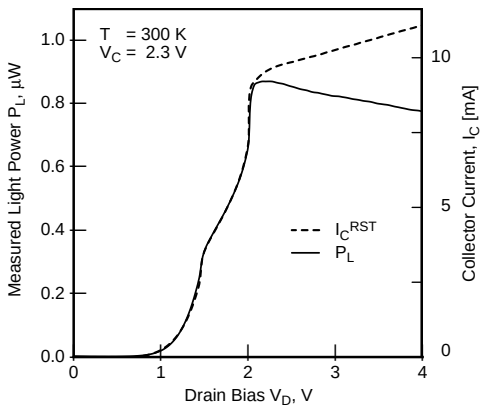

Fig. 14: Room-temperature light-voltage characteristics of a single-channel $\tilde{3} \to 1$ at a fixed collector bias $V_C = 2.3\,V$. Electrode $\tilde{3}$ is grounded and 1 acts as the drain. Electrodes 2 and 3 are kept floating. The dashed line indicates the I_C^{RST} curve, obtained by subtracting I_C^{LKG} from I_C in Fig. 8.

5. REAL SPACE TRANSFER LOGIC

The symmetry equivalence (1) between the internal states $\mathcal{S}[V_D, V_C]$ of a CHINT device implies that its output optical power, which is proportional to I_C^{RST} and is controlled by the heating bias V_{DS}, is invariant if the potentials on the source and drain terminals are interchanged. Thus the device exhibits an exclusive-OR dependence of the emitted light power on the input voltages V_S and V_D, regarded as binary (high/low) logic signals.

Figures 15 demonstrate this logic operation at three different temperatures. The collector bias is fixed at $V_C = 3.0\,V$ and the input voltages are varied from $low = 0$ to $high = 1.5\,V$. Operation of an optical **xor** gate is illustrated in Fig. 15a. The data shown were obtained in DC measurements; no attempt was made to characterize the frequency response, as our device had not been designed for a fast operation. We see that the light-output power P_L obeys $P_L = \mathbf{xor}(V_S, V_D)$ at all temperatures, including room temperature. The slight asymmetry between the *on* states $(1,0)$ and $(0,1)$ indicates that our device is not perfectly symmetric due to processing variations. On the other hand, the difference between the *off* states $(0,0)$ and $(1,1)$ at high temperatures is owing to a

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space, cf. below: Figs. 22 and 26-30.

nonvanishing radiation associated with the leakage current.

It should be stressed that the low radiative efficiency associated with the leakage current is crucial for a successful **xor** operation of our device. For comparison, Fig. 15b shows the electrical behavior of our device at similar temperatures and biasing conditions. While the approximate symmetry between the *on* states $(1,0)$ and $(0,1)$ is well maintained, the function $I_C = \mathbf{xor}(V_S, V_D)$ obtains only at cryogenic temperatures. At higher T, the leakage of holes in the state $(0,0)$ makes it effectively an *on* state and the resulting function looks more like a **nand** than a **xor**.

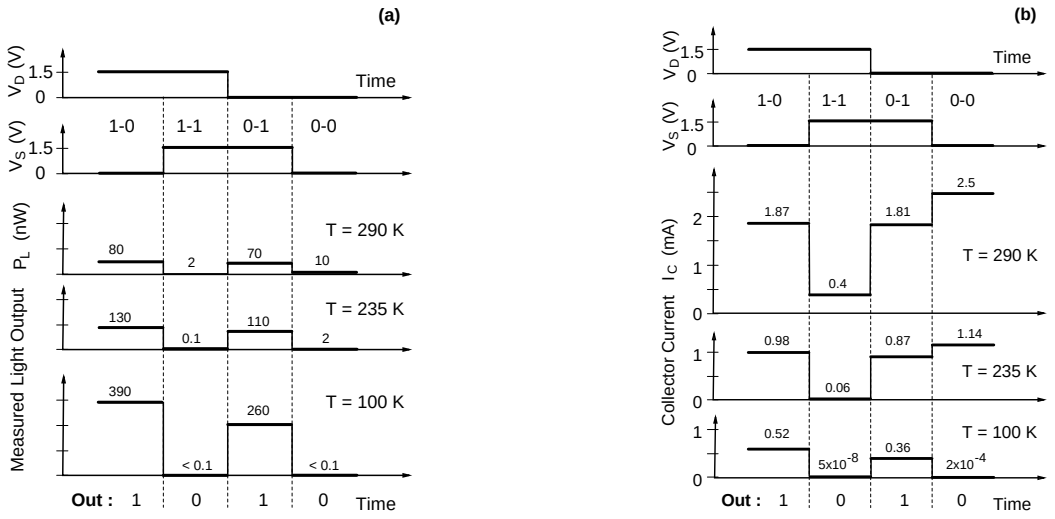


Fig. 15: Comparison of the optical and electrical logic operation of the complementary CHINT at different temperatures T. Four logic states $(1-0)$, $(1-1)$, $(0-1)$, and $(0-0)$ correspond to the electrical inputs $(V_S - V_D)$ taking the values $V = 0$ (logic-0) and $V = 1.5\,V$ (logic-1).
(a) Optical output, P_L, corresponds to $\mathbf{xor}(V_S, V_D)$ at all T, including room temperature.
(b) Electrical output, I_C, is $\mathbf{xor}(V_S, V_D)$ only at cryogenic temperatures.

Let us briefly discuss another possible application of the light-emitting CHINT: an optical frequency doubler of the electrical input signal.† Consider the device response to a sinusoidal variation of the voltage V_D on one of the emitter electrodes, D, keeping the other electrode, S, grounded, $V_S = 0$. The light output for V_D varying in the range $-2\,\mathrm{V} < V_D < 2\,\mathrm{V}$ and several fixed values of V_C, is shown in Fig. 16a, and the response to a sinusoidal variation of V_D is illustrated in Fig. 16b. Note that in this situation, the D electrode during the half-period when $V_D < 0$ is actually the source so that the effective collector-to-source voltage is varied. Because of the gating action of the collector field, the characteristics are asymmetric. The output comes twice per period in uneven pulses. No small-signal operation of this device is possible, because of the finite magnitude of the heating voltage required to initiate a tangible RST.

The threshold nature of the RST frustrates small-signal applications of the CHINT symmetry (1). Nevertheless, Mensz et al.[8] reported a unipolar operation of the CHINT as an electric frequency doubler. By intentionally driving up the leakage level with a high collector bias, they found a regime where the total $I_C(V_D)$ characteristic appears parabolic. A natural question arises as regards to the possibility of obtaining an optical analog of such a small-signal frequency doubler. In our present structure this is impossible precisely because of the low radiative efficiency associated with the leakage

† Such an application had been suggested to one of us (SL) by Professor K. Iga in a private communication (1990).

of holes. Perhaps, such an operation can be achieved using heterostructures in which both the leakage and the RST would be mostly due to the same carrier type (e.g. in n-channel complementary CHINT implemented in InGaAs/InP, where $\Delta E_V > \Delta E_C$). Of course, in such a structure the *on/off* ratio would be the same in both light and current. To recover superiority of the optical over the electrical logic operation in a InGaAs/InP complementary CHINT, one would have to use a p-type emitter.

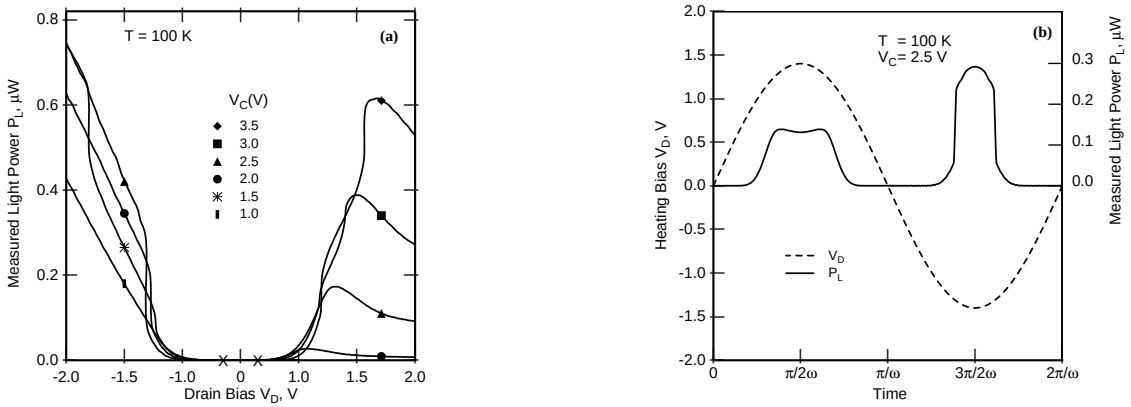


Fig. 16: Double-frequency optical pulse formation, illustrated at $T = 100\,\mathrm{K}$.
(a) Optical output for the heating voltage varying in the range $-2.0 < V_D < +2.0\,\mathrm{V}$ and several fixed collector biases. For a grounded S electrode and negative V_D, it is the D electrode that plays the role of a source. Note the broken voltage scale near $V_D = \pm 0.5\,\mathrm{V}$.
(b) Quasi-stationary evolution of the optical signal P_L (solid line) in response to a sinusoidal heating voltage V_D (dashed line).

5.1 ORNAND Logic

Since we set the periodic boundary conditions $\mathbf{V}_{\tilde{3}} = \mathbf{V}_3$, our multi-terminal device has effectively three input terminals. One of these can be viewed as a control electrode which determines which of the two logic functions **or** or **nand** is executed on the other two inputs. Choice of the control electrode is arbitrary. The collector current I_C and the light power P_L represent the logic output. We shall refer to the states with *high* and *low* values of the output as *on* and *off* states, respectively.

Figure 17 demonstrates the room-temperature logic operation of the ORNAND gate. The light signal has been detected from the back of the polished substrate using a microscope objective to collect the light. The substrate thickness has been polished down to $35\,\mu\mathrm{m}$ reducing the free carrier absorption in the substrate. The collector bias is fixed at $V_C = 2.4\,\mathrm{V}$ and the input signals $\mathbf{V}_1$ and $\mathbf{V}_2$ are varied between $low = 0$ and $high = 3\,\mathrm{V}$, while the split electrode, chosen as the control, is fixed either at the *low* value $\mathbf{V}_3 = 0$ for the **or** function or at the *high* value $\mathbf{V}_3 = 3\,\mathrm{V}$ for the **nand** function.

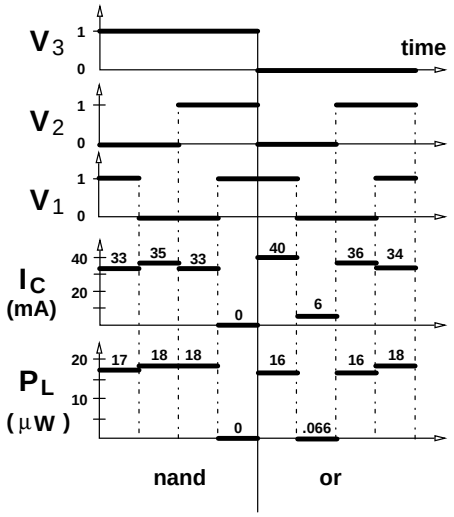
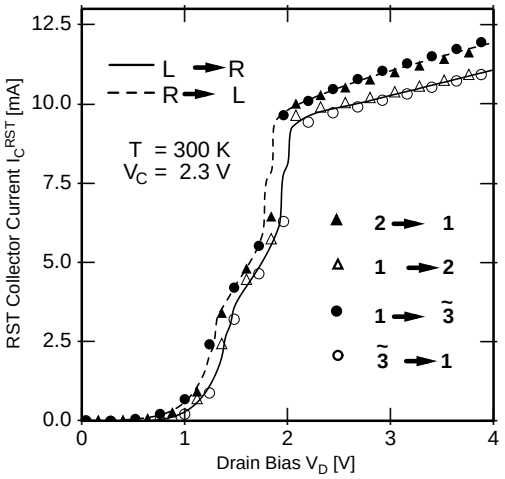


Fig. 17: Optical and electrical logic operation of the ORNAND gate, obtained in a quasi-stationary measurement at room temperature and $V_C = 2.4\,\mathrm{V}$. Electrodes 3 and $\tilde{3}$ are tied together. The binary values "logic-0" and "logic-1" of the input signals $\mathbf{V}_1$, $\mathbf{V}_2$, and $\mathbf{V}_3$ correspond to 0 and 3 V, respectively. The particular grouping of the states into OR and NAND reflects the choice of $\mathbf{V}_3$ as the "control" electrode.

As seen from Fig. 17, the symmetry between different *on* states is well maintained, both for I_C ($\pm 8\,\%$) and P_L ($\pm 6\,\%$). The larger variation in I_C is due to the variation in the leakage current of holes. Different *on* states correspond to different areas A_S of the source contact: A_S is 25 % of the total emitter area for **nand**(0,1) and **nand**(1,0), while $A_S = 75\,\%$ for **or**(0,1) and **or**(1,0), and $A_S = 50\,\%$ for **nand**(0,0) and **or**(1,1). The larger the source area the larger is the leakage current which is added to the RST current. Since the radiative efficiency of I_C^{LKG} is negligible compared to that of I_C^{RST}, the *on* states are more homogeneous in the measured light output. The low radiative efficiency of I_C^{LKG} also explains the fact that the *off* state of the **or** function is less than perfect electrically (the ratio $on/off \approx 7$ in I_C), while more than satisfactory optically ($on/off \gtrsim 200$ in P_L). In the *off* state there is no RST and most of leakage results from holes injected in the emitter layer.

Variation in the effective source area is not the only cause for violation of the basic symmetry Eq. (1). Another way to break this symmetry is to displace the channel-defining trench in the n^+ cap layer from its nominal position exactly in the middle between neighboring electrodes. Figure 18 shows the single-channel $I_C^{RST}(V_D)$ characteristics for two different channels and two different source→drain orientations. We see that the curves corresponding to the same orientation in two different channels coincide more closely than those for the same channel but different orientations. This observation holds true for all devices examined. We remark that the data in the present report have been collected from a wafer with an exceptionally lucky alignment of the trench and the source/drain metal masks. In other wafers, the difference between the RST in opposite orientations of the same channel is even larger. Nevertheless, this has no effect on the symmetry of *on* states in the ORNAND gate. Indeed, the symmetry break due to a trench misalignment has to be identical in all the three channels, cf. Fig. 2b. Noting that each of the six *on* states has two channels under field − one of each orientation − we see that the systematic asymmetry cancels out in the ORNAND logic operation, cf. the Table in Fig. 18.



input V_1, V_2	0, 1	0, 0	1, 0	1, 1
or $V_3 = 0$	1 ➔ 2 3 ➔ 2	/	$\tilde{3}$ ➔ 1 2 ➔ 1	$\tilde{3}$ ➔ 1 3 ➔ 2
nand $V_3 = 1$	1 ➔ $\tilde{3}$ 1 ➔ 2	1 ➔ $\tilde{3}$ 2 ➔ 3	2 ➔ 1 2 ➔ 3	/

Fig. 18: Asymmetry due to the misalignment of trenches in the ORNAND gate of Fig. 2b. The arrow indicates the source→drain orientation and its position the trench misalignment. Thus, the symbol $S \rightarrow D$ indicates that the trench is closer to the drain (D) electrode. The figure shows a comparison of the RST for two opposite orientations of the channel field in two different channels. The leakage current I_C^{LKG} is subtracted, as in Fig. 14. The table on the right indicates the working channels, i.e. those channels that are under the heating field in all logic states of the gate.

6. HOT-ELECTRON INSTABILITIES AND COLLECTOR-CONTROLLED STATES

As we have seen above, the *IV* characteristics of charge injection transistors are extremely nonlinear, including a strong negative differential resistance (NDR) in the $I_D(V_D)$ dependence with sharp steps, cf., e.g., Fig. 6 or 8. Monte Carlo (MC) simulations[21,22] of the CHINT, demonstrate internal switching and the formation of high-field domains. These instabilities arise due to a positive feedback between the RST and the heating electric field in the emitter channel. Both experimental measurements and MC calculations have been limited in analyzing RST effects due to the restriction of tracing *IV* characteristics exclusively in voltage increments. Significant progress in the understanding of the RST instabilities was achieved[9,23] with the help of continuation modeling and transient device simulation.

The study of hot-electron domains in RST transistors is important for understanding device limitations. Switching of the electron-heating control to the collector restricts the range where CHINT can be used as a linear amplifier. The frequency performance of CHINT in its usual mode is believed to be limited only by the time of flight of hot electrons over high-field regions of the device, i.e., over distances of order the barrier-layer thickness. The cutoff frequencies, extrapolated from the microwave measurements[24] of scattering parameters in a unipolar CHINT structure with a 2,000 Å-thick barrier, were 40 Ghz for both the current and the power gain. the transit time can be estimated to be of order 2-3 ps, which sets the upper limit for unity-gain cutoff frequencies at around 50 GHz. The ultimate speed performance can be achieved with an inverted CHINT structure in which the collector is the top layer.[25–27] This allows a reduction of the parasitic drain-collector capacitance and therefore the use of narrower barriers. With sufficiently narrow barriers, the CHINT can be expected to outperform a field-effect transistor of similar geometry (the RST collector corresponding to the FET gate, etc.) because the small-signal performance of CHINT is not limited[1] by the time of flight between the source and the drain. This advantage was recently demonstrated experimentally.[26] However, the domain formation itself seems to be a longer, FET-like, process, cf. Figs. 20 and 25 below.

Results of the numerical simulation[9,23] of the hot-electron transport in a three-terminal RST structure are reviewed below. A number of two-dimensional simulations of a unipolar CHINT have been performed, varying the device geometry (channel length L_{CH} and barrier thickness d_B), transport parameters, and the external bias conditions. Both stationary and time-dependent problems have been investigated.

6.1 Mathematical Model

Any model which attempts to account for real-space transfer effects must directly include terms for carrier heating. Further, the ability to specify some form of Neumann boundary conditions is essential for tracing arbitrary, multivalued *IV* characteristics. Both of these requirements are met by the general-purpose device simulator PADRE[28] which solves partial differential equations derived from moments of the Boltzmann equation. Simulations described below employed an energy balance system[29,30], defined in terms of the electrostatic potential ψ, the electron density n, and the electron temperature T_e. Precise equations used are listed elsewhere.[31]

Through an element-based data structure, PADRE decomposes a device domain into arbitrary, nonplanar configurations of regions; for instance, any number of heterointerfaces can terminate abruptly at a single location (node). Data at the vertices of each element can have local material and model dependencies. The impurity concentration and solution variables are allowed to change abruptly across any heterostructure interface. In this analysis, the quasi-Fermi level and T_e are assumed continuous, thus introducing a T_e dependence in the interface condition on local electron density n; this means that the RST current density at energy barriers is thermionic and included self-consistently.

Models for μ and τ_e as a function of T_e are typically derived from user-defined (e.g. MC) velocity-field $v(F)$ and temperature-field $T_e(F)$ relations for homogeneous slabs. To avoid confusion with negative differential mobility effects arising from momentum space transfer, a single population of electrons has been used with a monotonic $v(F) = \mu_0 F\,[1 + (\mu_0 F/v_{sat})^2]^{-1/2}$ relation[32] together with the $T_e(F)$ implied by a T_e-independent diffusivity.[33] All the results remain qualitatively similar for more realistic $v(F)$ and $T_e(F)$. For similar reasons, impact ionization and tunneling effects were excluded. Other parameters were selected to match the InGaAs/InAlAs system as exactly as possible.

In order to trace the complex IV curves shown below, it is necessary to apply mixed current/voltage boundary conditions. The predictor-corrector continuation method[34] based on a pseudo-arclength σ was used for this purpose. Computationally, the continuation method requires the addition of a single algebraic auxiliary equation, typically written in terms of the voltage and current (V_j, I_j) and the unit tangent $(\dot{V}_j, \dot{I}_j)$ at a known point on the curve j. The unit tangent can also be used to detect limit points (e.g. where $\dot{V} = 0$ or $\dot{I} = 0$) and to predict an initial guess for the subsequent bias point $j+1$. Figure 19 illustrates the continuation method and associated auxiliary condition on the pseudo-arclength used here.

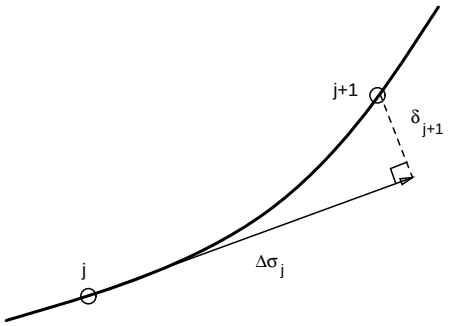


Fig. 19: Predictor-corrector continuation[34] applied to step between consecutive points j and $j+1$ on an IV curve. The

$$\dot{I}_j\,(I - I_j) + \dot{V}_j\,(V - V_j) - \Delta\sigma_j = 0$$

where the next pseudo-arclength step $\Delta\sigma_{j+1}$ is automatically controlled by a user-specified tolerance on the error of the tangential projection δ_j.

6.2 Broken Symmetry and Formation of RST Domains

Rapid Ramping. Figure 20 illustrates a time-dependent simulation of a device with $L_{CH} = 5\,\mu m$ and $d_B = 0.2\,\mu m$. Both S and D electrodes are kept grounded, while V_C is linearly ramped from 0 to $V_C = 2\,V$. Depending on the ramping time τ the device settles in one of two states: for $\tau > \tau_{cr}$ it is the normal† state, whereas for $\tau < \tau_{cr}$ the steady state carries a large RST current (Fig. 20a). The critical ramping speed is determined by the rate at which the increasing fringing field (Fig. 20b) is screened by channel electrons. The value of $\tau_{cr} \simeq 32.3\,ps$ roughly corresponds to the time of electron travel from S and D contacts to the middle of the channel.

The anomalous state at $V_D = 0$ exists only for a sufficiently high V_C, and the value of V_C^{cr}, below which this state disappears, depends on the device geometry and v_{sat}. The value of V_C^{cr} is sharply defined, and for the ramp end voltage V above V_C^{cr}, one has $\tau_{cr} \propto V$ to a good approximation, cf. Fig. 21a. This indicates that the relevant critical parameter is the displacement current ($\propto dV/dt$), which should be compared to a transient current ($\propto v_{sat}$) associated with electron screening processes in the emitter.

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† In a "normal" state of the device, for $V_{DS} = 0$, the collector draws only a minimal current, determined by the barrier height and the temperature. In this state a variation of V_C has the sole effect of changing capacitively, as in a field-effect transistor, the electron concentration in the channel.

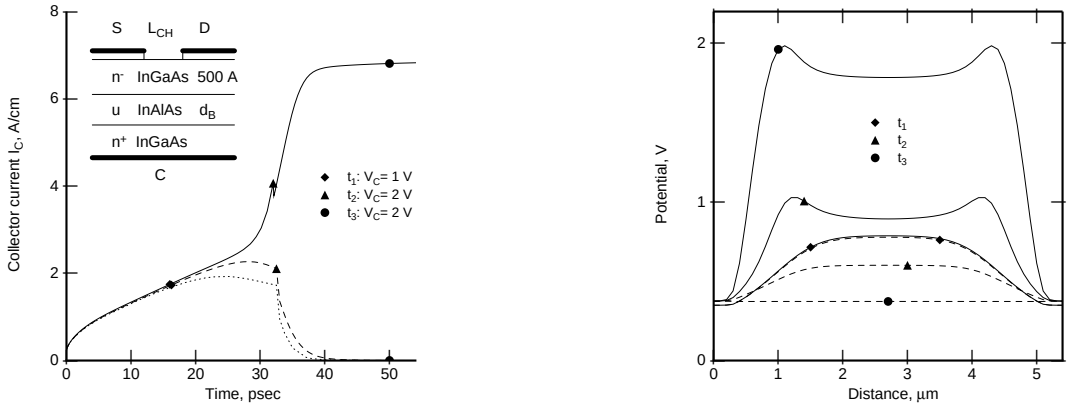


Fig. 20. Time-dependent simulation of a real-space transfer transistor with $L_{CH} = 5\,\mu\text{m}$, $d_B = 0.2\,\mu\text{m}$, and $v_{sat} = 10^7\,\text{cm/s}$. The collector voltage is ramped linearly from $V_C = 0$ at $t = 0$ to $V = 2\,\text{V}$ at $t = \tau$. The results are plotted for two situations: $\tau = 32.0\,\text{ps} < \tau_{cr}$ (solid lines) and $\tau = 32.5\,\text{ps} > \tau_{cr}$ (dashed lines).
(a) *left figure*: Collector current $I_C(t)$; inset shows cross-section of the device structure. Dotted curve corresponds to the absence of a RST (pure displacement current); it is obtained by artificially increasing the barrier height.
(b) *right figure*: Potential distribution $V(x)$ along the channel at selected times.

The values of τ_{cr}, determined to within $0.1\,\text{ps}$, are plotted in Fig. 21b against the emitter channel length L_{CH} for different assumed values of v_{sat}, barrier thicknesses, and ramp end voltages V. For short L_{CH} the dependence $\tau_{cr}(L_{CH})$ is approximately quadratic, and for long L_{CH} the dependence is linear.

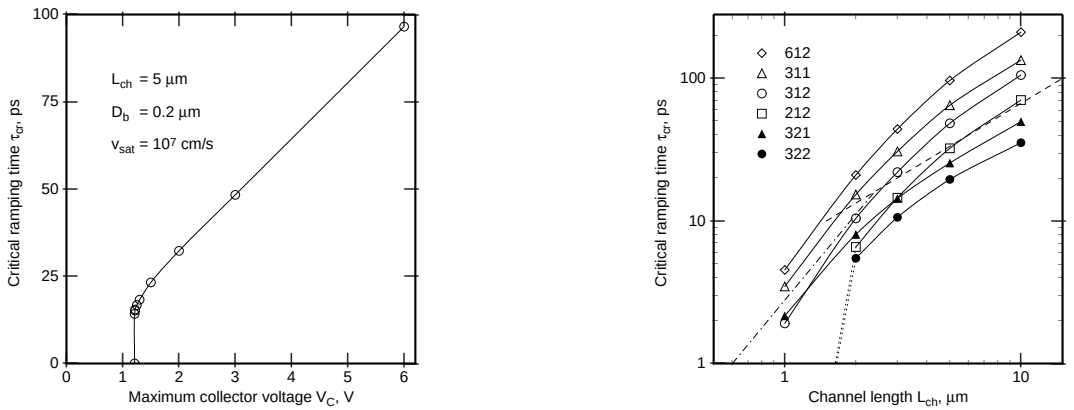


Fig. 21. Critical ramping speed for the formation of a stable anomalous stable state at $V_D = 0$. The collector bias is ramped linearly $V_C = 0 \to V$ in the time interval τ. For $\tau > \tau_{cr}$ the device settles in the normal state, for $\tau < \tau_{cr}$ in the anomalous state (**d** in the notation of Fig. 22).
Left figure: Dependence of τ_{cr} on the endramp voltage for a $5\,\mu\text{m}$ device. $V_C^{cr} = 1.21\,\text{V}$.
Right figure: Curve labels *VSD* indicate the endramp voltage (V) in volts, the saturated velocity (S) in $10^7\,\text{cm/s}$ and the barrier thickness (D) in $1000\,\text{Å}$. The dashed and stipple lines indicate linear and quadratic dependences, respectively.

Stationary Characteristics. Starting from the two stationary states at $V_D = 0$, it is possible to determine the characteristics $I_D(V_D)$ and $I_C(V_D)$ at a fixed collector voltage $V_C = 2\,\text{V}$ relative to the S electrode. With the predictor-corrector continuation method[34], one can trace arbitrarily shaped, connected components of the characteristic, starting from any established state within each component. The curves in Fig. 22 correspond to the locus

of points in the (V_D, I_D) plane for which the device has a steady state at a given V_C. To our knowledge, the displayed $I_D(V_D)$ dependence represents the first example of a multiply connected current-voltage characteristic. Any transition between disconnected components of the graph requires a global redistribution of the state fields corresponding to the formation or repositioning of high-field, high-temperature domains in the structure. Such a redistribution, reminiscent of a phase transition, is forced as V_D increases beyond the rightmost point (**k**) of the bounded graph component.

The potential profiles $V(x)$ along the channel − before and after the transition − are shown in Fig. 23. Of the three collector-controlled states, **s**, **t**, and **u**, corresponding to the same ($V_D \approx 0.82$ V) external bias as the state **k**, two (**s** and **u**) are stable. The actual transition occurs into the state **u** which has the highest value of the collector current. This has been ascertained by a time-dependent simulation in which the initial state **k** was perturbed by a small step $V_D(\mathbf{k}) \rightarrow V_D(\mathbf{k}) + \delta V_D$. The hot-electron domains in the state **u** are characterized by a strong field concentration, accompanied by a dramatic rise in T_e. The electron concentration in the domain is depleted so that the collector field remains unscreened and the local potential goes below that of the drain, resulting in a negative I_D. All states on the **p** – **u** – **d** branch of the collector-controlled component are similar to **u** and perfectly stable.

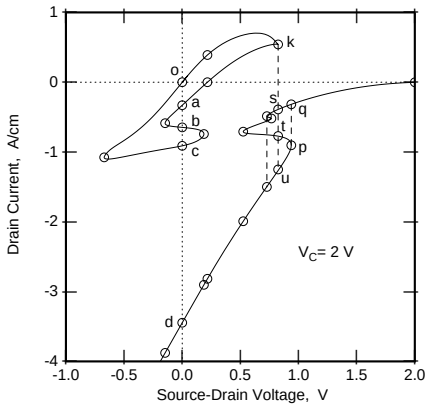


Fig. 22. Current-voltage characteristics obtained by the continuation method.

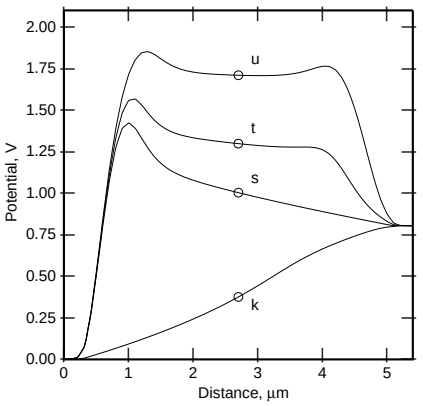


Fig. 23. The channel potential profile $V(x)$ in different CHINT states at the same external bias ($V_C = 2$ V, $V_D = 0.825$ V).

This indicates that state **d** (which we had first found in rapid ramping of V_C at $V_D = 0$, cf. Fig. 20) is experimentally accessible by a quasi-static variation of V_D at fixed V_C. The existence of a stable anomalous state **d** is obviously a necessary (though insufficient) condition for the multiply-connected topology of the $I_D(V_D)$ characteristic. As discussed above, it results when the competition between RST and screening of the fringing collector field is resolved in favor of RST. Precisely when this happens depends on the transport parameters assumed and the device geometry.

Unstable anomalous states. In addition to the normal state **o** and the anomalous state **d**, Fig. 22 reveals three other anomalous states (**a**, **b**, and **c**) at $V_D = 0$. The profiles $V(x)$ along the channel in these states are shown in Fig. 24.

It is clear that because of the non-linear nature of the problem, the actual stationary states may not transform according to irreducible representations of the symmetry group of the equations governing the device behavior at $V_D = 0$. The distribution of internal fields in the anomalous states is either fully symmetric or these states form a set of partners and transform into one another under the symmetry operations. Thus, states **a** and **c** under reflection transform into each other, even though the group has only one-dimensional linear representations. On the other hand, states **o**, **b**, and **d** are symmetric. Biasing the D electrode with respect to S breaks the reflection symmetry and allows a continuous transformation between states of different symmetry

on the loop.

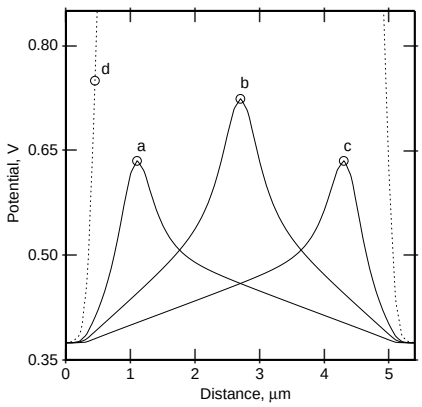
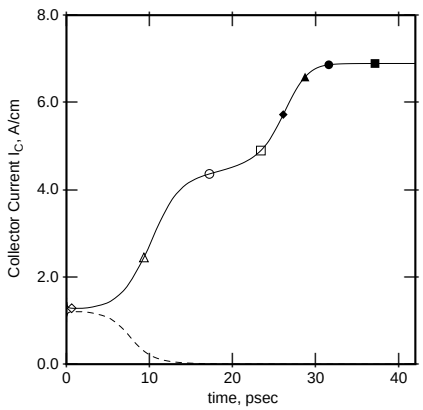


Fig. 24. The channel potential in the four anomalous states at $V_D = 0$.

Of the five states at $V_D = 0$ and $V_C = 2\,\mathrm{V}$, only two (**o** and **d**) are stable with respect to small perturbations. This has been ascertained by following the evolution of states in the vicinity of the steady states at $V_D = 0$. In these simulations, Fig. 25, the initial states $\mathbf{a}_\pm$, $\mathbf{b}_\pm$, and $\mathbf{c}_\pm$ have been assumed to coincide with a state on the loop displaced from **a**, **b**, and **c**, respectively, by an infinitesimal voltage $\delta V_D = \pm 10\,\mathrm{mV}$. Even though these states are virtually indistinguishable from the corresponding stationary ones, we found that $\mathbf{a}_+$, $\mathbf{b}_-$, and $\mathbf{c}_-$ evolved into **o**, while $\mathbf{a}_-$, $\mathbf{b}_+$, and $\mathbf{c}_+$ into **d**. All these instabilities develop on a rapid time scale, corresponding to the electron travel over the distances of the order of the domain size. They result in either the formation (repositioning) of a hot-electron domain, or its complete quench due to the screening by channel electrons.



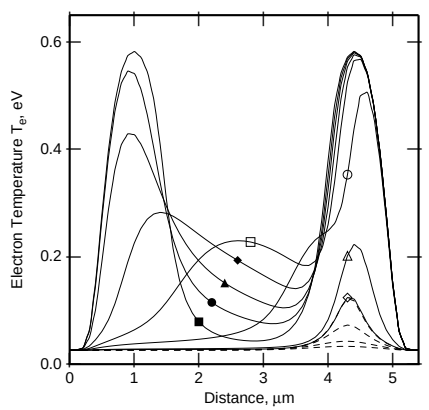


Fig. 25. Evolution of the non-stationary states $\mathbf{c}_+$ (solid lines) and $\mathbf{c}_-$ (dashed lines) at $V_D = 0$. Time dependence of the injection current is shown in *the left figure*; symbols mark the selected times in the evolution, at which the electron temperature profiles are plotted in *the right figure*. The "plateau" in the $I_C(t)$ dependence near $t = 20\,\mathrm{ps}$ evidently corresponds to the situation when a fully-developed hot-electron domain exists already near D but not yet near the S electrode.

Note that the question of stability of a given state can usually be ascertained *without* costly time-dependent simulations – by inspecting the phase diagrams $I_D(V_C,V_D)$ and $I_C(V_C,V_D)$ discussed below. The instability of states **a** and **c** is associated with a NDR in the $I_C(V_C)$ dependence, $\partial I_C/\partial V_C < 0$, and that of **b** with both $\partial I_C/\partial V_C < 0$ and $\partial I_D/\partial V_D < 0$. No counterexample to this rule has yet been found.

DC mappings of CHINT current-voltage characteristics. Fig. 26 shows $I_D(V_{DS})$ characteristics for a single device at $T = 300\,\mathrm{K}$ using a series of fixed collector voltages

(V_{CS}). Close examination of the characteristics shows numerous topological transformations. Beginning as an accumulation mode FET at low V_{CS} (<1.0V), the onset of RST initiates the formation of a slight NDR region in the $+V_{DS}$ direction (≈ 1.0V). At higher V_{CS}, separate folds begin to appear for both $V_{DS}>0$ and $V_{DS}<0$, although the curves remain singly connected. At $V_{CS}\approx 1.2$V, a disconnected loop begins to appear in the left-hand plane, corresponding to a surface bounded by a minimum V_{CS} in the 3D space in Fig. 26. As shown in Fig. 27 ($V_{CS}=1.5$V), this closed loop and the needle-like fold emanating from the bottom of the left-hand plane both continue to open, and the ''S-shaped'' notch in the right-hand plane (the knee reached by tracing backwards from $V_{DS}=+\infty$) moves leftward as V_{CS} increases. By $V_{CS}=1.6$V, the characteristic is transformed into a loop which includes the origin, and a singly connected component which is multivalued but has no folds or intersections with the loop. These two components maintain essentially the same topology for larger V_{CS} although their separation in (I,V) increases, cf. Fig. 22.

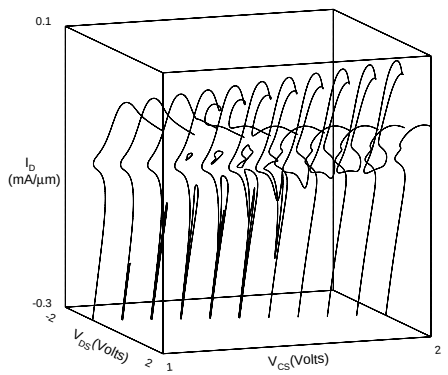


Fig. 26: CHINT I_D-V_{DS} characteristics for $1.0\text{V}\le V_{CS}\le 2.0\text{V}$ ($L_{CH}=5\mu$m, $d_B=0.2\mu$m, $v_{sat}=1\times10^7$cm/s). Curves represent simulations at constant V_{CS} separated by $\Delta V_{CS}=0.1$V.

Note the multiplicity of anomalous $V_{DS}=0$ states. In general, at $V_{DS}=0$, we can expect an odd number m_S of symmetric states and an even number m_A of asymmetric ones, because there should always be one and only one unbounded path in the (V_{DS},I_D) plane, while, by symmetry, asymmetric states come in pairs. Varying V_{CS}, we have been able to realize cases with $(m_S,m_A)=(1,0),(3,0),(3,2),(3,4)$, and $(5,4)$. In a continuous variation of V_{CS} one can, of course, arrive at a situation when the $I_D(V_{DS})$ curve only touches the $V_{DS}=0$ axis without crossing. At this singular point there is an accidental degeneracy of two symmetric states, and the total number of distinct symmetric states becomes even.

Interestingly the symmetry partners may belong to topologically disconnected branches of the I_D–V_{DS} characteristic. It is in fact the existence of unpaired asymmetric states along the singly connected, outer curve in Fig. 27 that has led[23] to the discovery of the loop, disconnected from the origin.

Figure 28 shows a map of the I_C-V_{DS}, corresponding to the I_D-V_{DS} plot in Figs. 27. Together, they completely define the device state since $I_C=I_S+I_D$. Although slices of I_C-V_{DS} space for a given V_{CS} are not symmetric, there is symmetry in the 3D space, expressed by Eq. (1). Since the collector current is invariant under the symmetry transformation, plots of I_C-V_{DS} have many self-intersections, cf. Fig. 28. Points defined by a single intersection with the $V_{DS}=0$ axis correspond to symmetric states ($I_C=2I_D=2I_S$); points defined by two coincident intersections represent reflective, asymmetric pairs.

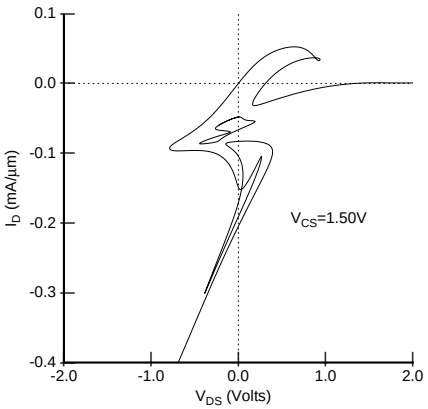


Fig. 27: Single CHINT I_D-V_{DS} characteristic from Fig. 26 for $V_{CS} = 1.50\,\mathrm{V}$ which contains both a self-intersecting component and a disconnected loop.

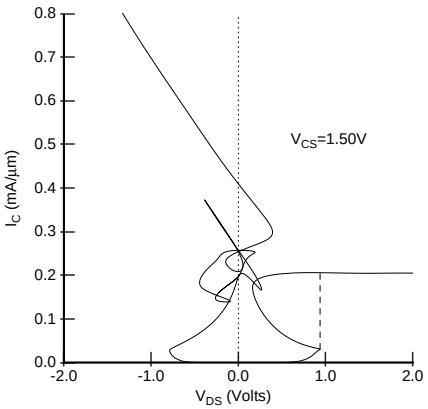


Fig. 28: Single CHINT I_C-V_{DS} characteristic for $V_{CS} = 1.50\,\mathrm{V}$ corresponding to the I_D-V_{DS} in Fig. 27.

Phase space mappings, like those represented by curves in Figs. 27 and 28, have the property that except in the vicinity of self-intersections, their infinitesimally close points correspond to infinitesimally close state vectors $\mathbf{z} \in \boldsymbol{R}$ in the multidimensional space $\boldsymbol{R}$, describing the state of the device [i.e. all the fields $n\,(x,y)$, $T_e(x,y)$, $\psi(x,y)$, etc.]. The converse is always true: points separated by a finite distance on a (V,I) plane correspond to macroscopically distinct states $\mathbf{z}$. Continuation in the pseudo-arclength produces a completely smooth evolution of the device state. In contrast, experimental measurements (and MC simulations) force abrupt transitions at limit points, for instance $\mathbf{k}\rightarrow\mathbf{u}$ in Figs. 22, as V_{DS} is increased from 0, corresponding to the formation or repositioning of a high-field, high-temperature domain. The resultant negative I_D at $\mathbf{u}$ arises as the potential in the hot electron domain is lower than that of the drain, due to the unscreened collector field.

Fig. 29 shows the results of continuation simulations started from the origin for $V_{DS} > 0$, using a higher saturation velocity v_{sat}. Both the V_{CS} and V_{DS} thresholds for causing folds or limit points in IV increase with v_{sat}. The thresholds are reduced for smaller L_{CH}, see Fig. 30. These dependencies are similar to those described above in connection with the critical ramp speed of a transient V_{CS} excitation required to induce the stable $\mathbf{d}$ state at $V_{DS} = 0$.

In spite of the somewhat artificial $v(F)$ and $T_e(F)$ assumed in the simulation, it can be safely concluded that the cause of the nonlinear steps observed past the RST threshold in experiments are the loops and folds predicted by continuation. Transient simulations corresponding to measurement procedures indicate that folds (e.g. in Fig. 29 for $V_{CS} = 3.0\,\mathrm{V}$) can be followed to some length. Predictions of where the state transition will occur can be extracted accurately from complete dc IV maps, but this analysis must include consideration of NDR effects at all terminals as well as external circuit configurations.†

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† It would be very interesting to understand what is the physical basis for the continuity of W_{tot} noted empirically at many transitions in experimental CHINT characteristics, see Fig. 13b and the footnote below Eq. (6).

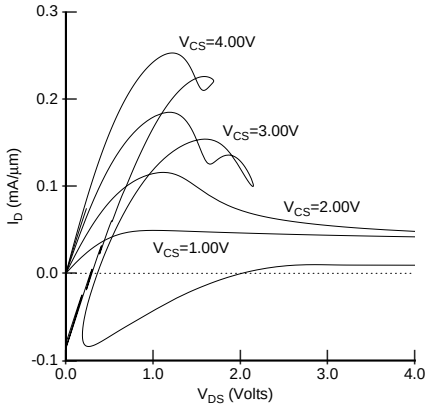

Fig. 29: CHINT I_D-V_{DS} characteristics as a function of V_{CS} ($L_{CH} = 5\,\mu m$, $d_B = 0.2\,\mu m$, $v_{sat} = 2\times10^7$ cm/s). Results are shown only for the $V_{DS} > 0$ branches initiated from the origin.

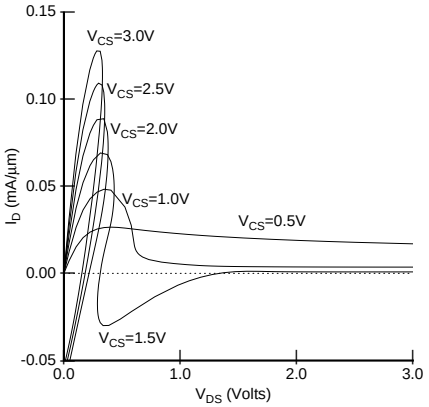

Fig. 30: CHINT I_D-V_{DS} characteristics as a function of V_{CS} ($L_{CH} = 2\,\mu m$, $d_B = 0.2\,\mu m$, $v_{sat} = 1\times10^7$ cm/s). Results are shown only for the $V_{DS} > 0$ branches initiated from the origin.

6.3 Summary of the Simulation Results

The charge injection transistors possess complicated − often multiply-connected − *IV* characteristics. Application of a sufficiently high V_{DS} at a fixed $V_{CS} > 0$ forces a switching transition, accompanied by the formation of a hot electron domain. Physically, the domains form when the finite supply rate of electrons to a "hot spot" is exceeded by the RST flux from that spot. The depleted domains unscreen the fringing field ("normally" screened by channel electrons) and the RST becomes collector controlled.

Potential applications of RST devices are likely to be based on their peculiar symmetry with respect to the heating field polarity. The same symmetry shows up in the analysis of the hot-electron domain formation. States of a multiterminal RST device under general bias are "adiabatically" connected to the anomalous states of the symmetric configuration at $V_D = 0$. The symmetry analysis is likely to prove very potent with devices of more complicated geometry, such as the ORNAND gate of Fig. 2b, whose symmetry group is C_{3v}. Phenomena that occur at $V_{DS} = 0$ capture the essential physics associated with the RST domains in general.

The simulations described above have been carried out using a transport model which eliminates the usual instabilities resulting from a negative differential mobility (the latter has been artificially excluded). The results have been verified[23] to remain qualitatively valid with a more realistic velocity-field model appropriate for InGaAs. For a quantitative simulation of a particular RST device structure, like those in Fig. 2, one would clearly need a realistic transport model. However, the novel anomalies discussed in Sect. 6, can be qualitatively reproduced in *any* model that allows channel electrons to be heated and self-consistently includes the RST flux.

An essential feature of the above analysis is the use of continuation methods which allow the inspection of the full device phase space. Slicing the $I_D(V_D, V_C)$ surface at different V_C results in $I_D(V_D)$ curves of different topologies. The internal fields evolve smoothly along a connected $I_D(V_D)$ trajectory and do not signal the approach of a switching transition. Phase-space mappings successfully give the global type of information. Moreover, they usually give an unerring guess as to the *stability* of a given state, subsequently supported by costlier transient simulations. The understanding gained in this fashion will be invaluable in the application of RST transistors to the design of high-performance systems.

7. CONCLUSION

We have discussed the principle and the implementation of novel leight-emitting logic devices, based on the real-space transfer of hot-electrons between independently contacted complementary layers. A monolithic multiterminal logic device, that functions both optically and electrically as an ORNAND gate, has been described. The device, implemented in an InGaAs/InAlAs/InGaAs heterostructure, exhibits both the **or** and the **nand** functions of any two of the three input terminals. in either the output current or the optical output power. These functions are not fixed by the layout but are interchangeable by the voltage on the third ("control") terminal. Choice of the control electrode is, moreover, arbitrary. This is a unique logic device with such powerful capabilities; its function is electrically reprogrammable in the course of a circuit operation.

In the heterostructure used the valence band discontinuity is much smaller than that in the conduction band and most of the parasitic non-RST current is due to the injection of holes from the p-type collector layer into the n-type emitter. Due to a specially designed collector structure with a wide-gap InAlAs layer confining the active InGaAs layer, the radiative efficiency of minority carriers in the collector is much higher than that in the emitter. This makes the leakage current relatively non-radiative and substantially enhances the optical logic performance at room temperature.

The demonstrated device is an incoherent light-emitting source, similar to a conventional LED. In order to increase its output power and improve the frequency performance, we must take advantage of the stimulated emission in a resonant optical cavity. The high injection current density, $J_C \gtrsim 25\,\mathrm{kA/cm^2}$, obtained in the present device and its high internal radiative efficiency, comparable to that in conventional long wavelength LED's, are promising for the future implementation of a real-space transfer logic laser.

Both electrically and optically, the RST logic devices show a complicated nonlinear behavior, including a variety of novel instabilities, in the internal state dependences on the input voltages. Much work is required, both experimental and theoretical, to use these instabilities in a controlled fashion for the implementation of fast functional devices.

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