Quasi-ballistic transport in nano-MOSFETs

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The International Roadmap for Semiconductors has predicted that starting from the 45-nm technology node, an increase of basic transport properties must be achieved to reach the specs of high-performance devices ("ballistic technology booster").[1] The on-current I_{ON} of a MOSFET is limited to a maximum value I_{BL} that is reached in the ballistic transport regime.[2,3] Hence, improvements of I_{ON} demand an increase of either I_{BL} or of the ballisticity ratio BR = I_{ON}/I_{BL} which is a metric of how close to its upper limit is the on-current of the device. The values of BR have not significantly improved in recent technologies[4] and are thought to have a modest dependence on the technology node and on the gate length L_G for conventional silicon MOSFETs. Further improvements in I_{BL} requires ultra-thin body (UTB) silicon-on-insulator with silicon thickness below 10 nm or non-conventional channel composition.[5]

We have extended previous analyses of the role of scattering in the channel and in the drain of decananometer MOSFETs and our results demonstrate that, for the explored L_G values, the scattering still controls the on-current and keeps it much lower than the ballistic limit.[6] We have also compared the results of Monte Carlo (MC) simulations to analytical models for quasi-ballistic transport available in the literature.[2,3] These models provide useful physical insight as they correctly link the achievable on-current to the scattering events taking place in the channel region where a voltage drop equal to the thermal energy kT occurs (KT-layer). However, quantitative predictive analysis of the on-current in short MOSFETs would require a two-dimensional (2D) self-consistent simulation because the information concerning the position of the virtual-source (location of the potential-energy maximum), the extension of the KT-layer and the mean free path are not known *a priori*. Self-consistent MC simulation represents the ideal tool for this analysis, as it can handle the progressive transition from scattering-dominated transport to quasi-ballistic transport, that occurs as the channel length is scaled to values close to the carrier mean free path. In this framework, we present a systematic study of bulk and UTB double-gate MOSFETs designed according to the ITRS specs, in order to understand to which extent ballistic transport is going to affect devices with L_G down to 14 nm. The results point out that UTB double-gate MOSFETs get closer to the ballistic limit compared to bulk devices.

1. ITRS Roadmap 2004 Update Emerging Research Devices (ERD).
2. M. Lundstrom, *IEEE Electron Device Lett*. **18**, 361 (1997).
3. M. Lundstrom *et al.*, *IEEE Trans. Electron Dev*. **49**, 133 (2002).
4. M. Lundstrom, *IEDM Tech. Digest* 2003, pp. 789–792.
5. S. Takagi, *VLSI Symp. Tech. Digest* 2003, pp. 115–116.
6. P. Palestri *et al.*, *IEEE Trans. Electron Dev.* **52**, 2727 (2005).
7. S. Eminente *et al.*, *IEEE Trans. Electron Dev.* **52**, 2736 (2005).