Scaling limits of Si-CMOS and non-Si opportunities

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Scaling of CMOS and its limits has been a continuous subject for debates for a long time since as early as late 1970's. In some cases the limits were attributed to lithographic limitations, whereas in some other cases they were derived from some set of physical constraints under likely assumptions for device physics and process controllability for stochastic nature of parameters. However, up until now, either evolutionary or revolutionary breakthrough solutions were found resulting in enabling continuous scaling of CMOS up until now.

As we look at the future, it is more difficult to be as optimistic as we used to be, because a variety of issues and more importantly the magnitude of challenges which we can anticipate may not be as easily overcome as those of the past two decades. Not only difficulty in cost-effective processing equipment and process parameter controls, but also perceived limit in device operation improvement itself will depart from what we have experienced previously. At the device level, rapidly increasing leakage current of MOSFETs at the gate, drain/source terminals and less than expected improvement in the drive current with reduced channel length will prompt us to consider non-Si materials for the channel of MOSFETs. At the integration level, the interconnect delay which has been predicted as the stumbling block for high performance large chips will certainly become worse, coupled with power consumption and heat dissipation management challenges. As we will have more areas dedicated to high-speed embedded memory (mostly static random access), memory stand-by power will become a major problem with MOSFETs operated at much lower I_{ON}/I_{OFF} ratio than previously. Furthermore, general trends for system-on-a-chip driven by significant growth of wireless systems needs for mostly consumer products do require heterogeneous integration of digital, analog/RF, power management and more, making the magnitude of challenges worse than ever.

This talk will first discuss scaling trend of CMOS, coupled with possibility of new channel materials, metal gate/high-κ dielectric gate stacks and source/drain structures, followed by several possibilities and opportunities for non-Si devices, including new material-based non-volatile memory structures.