Negative bias temperature instability in SOI *p*–MOSFETs

Dimitris E. Ioannou and Dimitris P. Ioannou
George Mason University, U.S.A.

The negative bias temperature instability (NBTI) in *p*-MOSFET parameters (i.e., shifts in threshold voltage, saturation and subthreshold currents, transconductance *etc.*), which appear following the application of negative bias temperature stress, have reemerged recently as a major reliability concern for modern CMOS technologies.[1,2] This increased significance of NBTI is due to the fact that the gate oxide thickness scales faster than the power supply voltage, which results in an increasing oxide electric field with each successive technology generation. Additionally, the introduction of nitrogen in the gate oxide to control the gate leakage and boron penetration has been found to lead to increased NBTI for the same stress conditions.

NBTI reliability has not been studied as extensively in SOI technologies compared to bulk. However, due to the SOI structure itself (floating body, channel coupling, buried oxide quality, *etc*.) and perhaps more importantly, to the higher operating temperatures caused by the self heating effect, NBTI can be expected to be of even greater importance in SOI, and at the same time more difficult to study. In this poster we report results on NBTI tests for SOI MOSFETs selected from recent technologies designed for harsh environment (e.g., space, high temperature, *etc.*) applications.

We find that NBTI behaves very similarly or very differently in bulk and SOI *p*-MOSFETs, depending on the particulars of the SOI device structure and operation conditions. The most striking difference is observed when the SOI device operates under high gate and high drain bias, where self-heating causes significantly worse NBTI degradation in the SOI device. This is conventionally thought as the worst carrier stress for hot carrier injection (HCI) degradation, but it is shown here that in fact it is concurrent NBTI degradation instead: when studying "pure" NBTI degradation in SOI devices, the results are similar to bulk technologies, and in good agreement with the standard reaction-diffusion theory of NBTI. However, when both gate and drain are biased and the transistor conducts current, an interesting interaction of HCI and NBTI is observed, which leads us to resolve the question of worst case HCI stress conditions for *p*-channel SOI MOSFETs with thin gate oxides: we report that what had previously been thought as a shift of worst case stress HCI for deep sub-micron SOI PMOSFETs[3] to high gate/high drain voltage, from the conventional low gate/high drain voltage, is actually concurrent NBTI degradation.

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2. V. Huard *et al*., *J. Microelecron. Reliability*, in press (2006).
3. S.-H. Renn *et al*., *IEEE Trans. Electron Dev.* **45**, 2146 (1998).