Superconductor RSFQ microprocessors and systems:
Status, challenges, and projections

Mikhail Dorojevets
SUNY–Stony Brook, U.S.A.

Superconductor processors based on rapid single flux quantum (RSFQ) circuit technology can potentially reach and exceed operating frequencies of 100 GHz, while keeping processor power consumption low. The availability of ultra-high-speed, low power superconductor circuit technology is only one of several requirements for successful high-performance system design. In order to be able to initiate the design of a superconductor system for petaflops computing, the following critical design issues need to be addressed: processor microarchitecture, memory, and interconnect. The Superconducting Technology Assessment Panel convened by DoD conducted an assessment of the superconductor technology in 2005. The proposed development program plans to find and demonstrate viable solutions for these architectural, design, and fabrication challenges during the 2006-2010 time frame.

The key characteristics of superconductor processors, such as ultra-high clock frequency and very low power consumption, are due to the following properties:

- extremely fast (a few-picosecond) switching times of superconductor devices;
- very low dynamic power consumption of RSFQ gates;
- ultra-high-speed, superconducting interconnect capable of transmitting signals (picosecond pulses) with negligible attenuation at full processor speed.

While no radical execution paradigm shift is required for superconductor processors, several architectural and design challenges need to be addressed in order to exploit these new processing opportunities.

Most of the architectural and design challenges are not peculiar to superconductor circuitry but, rather, stem from the processor circuit speed itself. At the same time, some of the unique characteristics of the RSFQ logic will certainly influence the microarchitecture for superconductor processors.

The Superconducting Technology Assessment (STA) Panel conducted an assessment of the superconductor technology. The STA Panel developed a program with the estimated funding of ~ $350-400M to find and demonstrate viable solutions for architectural, design, and fabrication challenges during the 2006-2010 time frame.

The proposed program has two major goals for processor design:

- find viable microarchitectural solutions suitable for 50-100 GHz RSFQ processors;
- design, fabricate, and demonstrate a 50 GHz 32-bit 1-million gate processor with 128 KB, 200 GB/s off-chip local superconductor memory integrated on a multi-chip module.

It is also planned to develop a cell library and a set of CAD tools to allow engineers without deep knowledge of superconductivity to design superconductor circuits of such complexity and speed.

The proposed processor-memory demonstration is one of several targets set by the proposed five-year development program, which addresses a wide spectrum of design and fabrication issues in order to create a foundation for practical multi-petaflops superconductor system design.