Device Technology Rediscovers Market Reality?

Mark R. Pinto
Agere Systems, USA

Scaling of microelectronic devices has been driven by a variety of end application objectives. For VLSI-enabled products, the characteristics of the MOSFET and the size of investments enabled by the associated markets have been such that to date, progressive generations of technology have delivered improvements in almost every dimension – *e.g*. throughput, power, cost – enabling a broad array of successful products. However because VLSI scaling has neared a variety of limits (physics, materials, reliability, manufacturing), more compromises and tradeoffs have been necessitated, suggesting careful examination of appropriate technology R&D drivers. Issues like reliability and signal integrity cannot now be taken for granted. Further, the economics of masks, 300 mm wafers, high I/O packages, and testing also have significant impact on product directions.

On a related front, the ability to produce designs that take full advantage of underlying device technology advances has become more challenging. Numerous studies have shown that even with improved EDA tools, designer productivity lags transistor density improvement rates by a factor of 2–3. (And typically it is verification and validation as opposed to the design itself that occupies the bulk of the product development resources and schedule.) Differentiation of sub-100 nm processes may be prohibitively expensive to realize and furthermore can be counterproductive to product success – the race to deliver products is often won by those who can deliver the design IP first, and standard processes attract more (validated) building block IP with which to build systems chips.

Using primarily networking and communication applications – within the more realistic environment this industry segment now finds itself (i.e. not "bandwidth-at-any-cost") – this presentation will highlight the key VLSI technology directions and implications from a product and design perspective as we enter the sub-100 nm domain, hopefully continuing towards true digital nanotechnology.