The Future of CMOS Downscaling

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The recent trend of CMOS downsizing is very aggressive. Already L_G < 100 nm gate length MOSFETs have been introduced into production and a report of normal transistor operation of a 6 nm MOSFET was published in 2002. This L_G is already only 20 times larger than the Si atomic distance, so it is certainly true that the downsizing of MOSFETs is approaching its limits.

However, it is not necessary to become too pessimistic. It could still take 50 years for the L_G of LSI products to reach the atomic limit, even assuming that the past downsizing trends can be maintained. Of course, before reaching the ultimate atomic limit, downsizing will meet practical limits caused by one of the integration issues, such as chip performance, cost of development and production, power dissipation, reliability, yield, *etc*. Fortunately, chip performance is still expected to increase due to new technological developments and architectural improvements, until the L_G = 20 or 10 nm generation. Other integration issues do not seem to limit the downsizing in near future, although the rate of progress depends on the market and technology development.

Regarding the sub-10 nm region, unfortunately, there is no guarantee that L_G < 10 nm circuits will win in terms of performance, until good drain current drive of such MOSFETs is demonstrated. Drain currents of cutting-edge presented at recent conferences show significant degradation under the scaled supply voltages specified by the ITRS Roadmap. The main cause is expected to be the incompleteness of the MOSFET optimization, but there is no guarantee at this moment that the drain current of sub-10 nm MOSFETs will improve significantly in future.

Will L_G = 10 nm be the end of the downsizing? It is too early to conclude this. Silicon MOSFETs have been the smallest electronic device used in products for many years. With 1.5 nm gate oxides and 6 nm gate lengths at the research level, today's silicon ULSI MOSFET is clearly the most successful "nanodevice". No realistic replacement of silicon devices is apparent even after Si reaches its limits – whether at 20 atomic size length (6 nm) or single atomic size length (0.3 nm) – because other types of devices such as molecular transistors would also reach their downsizing limits.

One solution for the performance progress after or even before the downsizing limit is the integration of different functional chips. This kind of "system-on-a-chip technology" will reduce the huge parasitic packaging capacitances, save power and increase the performance. The functional chips can be silicon or non-silicon, and will be DRAM, SRAM, RF-device, lasers, *etc*.

Another solution might come from the system architecture or information processing algorithms. Comparing with biological system, the total performance of today's semiconductor computer is extremely low.

In regard to the cost issue, the required investment for the development and production of the chip keeps increasing for every new generation. Aggressive global alliance strategies between companies, including universities and government labs, will become the most important issue for the next 10 years in order to survive the downsizing race.