Silicon-on-Insulator (SOI): A Path for Integration of Silicon Light Emitters into Future Microelectronic Chips?

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Since demonstrating greatly enhanced light-emission efficiencies in bulk silicon light emitting diodes (LEDs),[1] our team has investigated prospects for applying these improvements to the co-integration of optical and electronic functions into silicon-based microelectronics.[2] The problem with efficient Si light emission is weak optical absorption, leading to long radiative lifetimes, pushing device design to large, slow devices for high efficiency. There might seem limited prospects for the high efficiency, compact devices required for microelectronics.

One mitigating factor is the perceived need for microelectronics to move to SOI to maintain present rates of progress, with particular benefits for ultra-thin (<10 nm) Si layers.[3,4] At these thicknesses, quantum confinement is important. Significantly for LEDs, absorption and radiative recombination rates also are expected to increase greatly, due to relaxation of momentum conservation and increased excitonic effects. To investigate further, we have studied optical properties of ultra-thin SOI (Fig. 1), with encouraging preliminary results. As Si thickness decreases, peak emission wavelength decreases due to confinement and, importantly, intensity also increases, confirming the expected increased absorption.

Such quantum confinement allows silicon's bandgap to be controlled by not only layer thickness, but also applied field (quantum-confined Stark effect). This allows high-speed modulation of Si LED output, as suggested by the CMOS compatible LED/modulator of Fig. 2. Variations in Si layer thickness within the chip also allow some regions to be transparent to emitted light and others opaque, adding to the attraction of the SOI microphotonics.

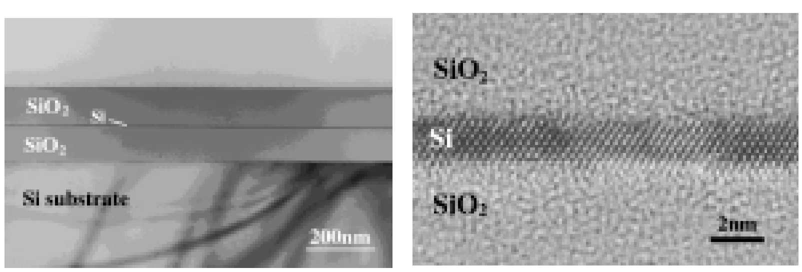

FIG. 1: Ultra-thin SOI: low (left) and high (right) magnification.

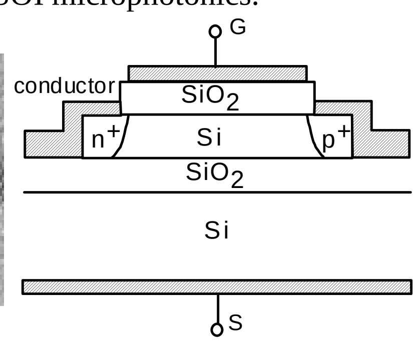

FIG. 2: Combined Si LED/modulator.

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1 M. A. Green *et al.*, "Efficient silicon light emitting diodes", *Nature* **412**, 805 (2001).

2 S. M. Sze, "Microelectronics technology: Challenges in the 21st century", in: *Future Trends in Microelectronics: The Nano Millennium,* New York: Wiley, 2002, pp. 3-16.

3 P. M. Solomon, "Strategies at the end of CMOS scaling", *ibid*., pp. 28-42.

4 D. Esseni *et al*., "Ultra-thin single- and double-gate MOSFETs for future ULSI applications", *ibid*., pp. 63-78.