SIMULATION OF MULTIPLY CONNECTED CURRENT-VOLTAGE CHARACTERISTICS IN CHARGE INJECTION TRANSISTORS

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ABSTRACT

Mappings of *IV* space for charge injection transistors are obtained from device simulations. Using transport models which self-consistently incorporate electron energy and real-space transfer currents over heterostructure interfaces, multiply connected, self-intersecting *IV* curves are obtained through the use of predictor-corrector continuation. These complex phase mappings help explain experimentally observed nonlinearities and suggest new regimes of device operation and application.

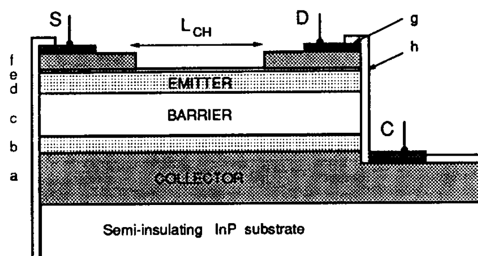
INTRODUCTION

The operation of the charge injection transistor or CHINT [1] is based on the principle of real-space transfer (RST) of electrons, heated by a lateral field, over an energy barrier. The symmetry of hot electron injection with respect to the heating field has lead to a number of practical applications including compact, multiterminal logic elements [2]. Experimental CHINT *IV* characteristics are extremely nonlinear, including a strong negative differential resistance (NDR) and sharp steps [3,4]. Previous attempts to simulate the CHINT, performed exclusively via Monte Carlo (MC) methods [5], have demonstrated internal switching and the formation of high-field domains. However the nonlinear characteristics are still not well understood.

The present work reports on InGaAs/InAlAs CHINT simulations performed via moment equations. Using powerful curve tracing algorithms, we have discovered what we believe to be the first occurrence of *multiply connected, self-intersecting IV curves* in an electronic device. In addition to providing an explanation for experimentally observed nonlinearities, these unique characteristics may lead to radically new functional device elements.

MATHEMATICAL MODEL

The analysis presented has been performed using the general-purpose (multicarrier, nonplanar, arbitrary materials) device simulator PADRE [6], which solves Poisson and carrier moment equations in 1, 2 or 3 spatial dimensions plus time. In order to account directly for electron heating, equations for energy transport [7,8] have been self-



a: 5000 Å InGaAs n^+ (Si:10^{19})
b: 500 Å InGaAs n^- (Si:10^{17})
c: t_B InAlAs u
d 500 Å InGaAs n (Si:10^{16})
e: 25 Å InAlAs n^+ (Si:10^{19})
f: 200 Å InGaAs n^+ (Sn:10^{20})
g: 500 Å Ti / 1000 Å Au
h: Si_3N_4

Figure 1:
Schematic of InGaAs/InAlAs CHINT used in this study. Geometric parameters which are varied include the channel length L_{CH} and barrier thickness t_B.

consistently included; see [6] for an exact formulation. Models for hot electron mobility and energy relaxation in each material system are given dependencies on the local electron temperature T_e, typically derived from user-defined (e.g. MC) velocity-field v(F) and temperature-field $T_e(F)$ relations for homogeneous slabs.

Through an element-based data structure, PADRE permits the decomposition of a domain into general, nonplanar configurations of regions; for instance, any number of heterointerfaces can terminate abruptly at a single location (node). In this analysis, the quasi-Fermi level and T_e are assumed continuous, thus introducing a T_e dependence in the interface condition on local electron density n; for Boltzmann statistics, this condition reduces to

$$n^{(m2)} = n^{(m1)} \frac{N_C^{(m2)}}{N_C^{(m1)}} \exp\left[-\frac{\Delta E_c(m2-m1)}{k\,T_e}\right]$$

at an interface between materials $m1$ and $m2$, where ΔE_c is the conduction band offset; a similar expression is implemented for more general distribution functions. These relations imply that the RST current density at energy barriers is thermionic and included self-consistently.

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To obtain complete mappings of CHINT IV space, predictor-corrector continuation methods [9] have been used. Instead of tracing IV characteristics by fixed ΔI or ΔV steps, these methods use a pseudo-arclength, varied automatically to meet a predefined error condition. For the arbitrarily complex graph components below, continuation proves essential in the discovery of new regimes of device operation. Continuation also helps to optimize nonlinear computational performance. Used within a full Newton method, reliable convergence is obtained throughout all bias configurations. Methods which incorporate nonlinear plug-in iteration (e.g. where T_e is held constant) have been found to fail in some CHINT operating regimes.

DC CHARACTERIZATION

A number of 2D CHINT simulations have been performed, varying the device geometry, transport parameters and bias conditions. Fig. 2 shows $I_D(V_{DS})$ characteristics for a single device at $T=300K$ using a series of fixed collector voltages (V_{CS}). To disentangle negative differential mobility effects arising from momentum-space transfer, a monotonic $v(F)=\mu_0 F[1+(\mu_0 F/v_{sat})^2]^{1/2}$ [10] has been employed together with the $T_e(F)$ implied by assuming a T_e-independent diffusivity [11]; the results remain qualitatively similar for more realistic $v(F)$, $T_e(F)$. Other parameters were chosen to be as representative as possible of the InGaAs/InAlAs system. In particular, the barrier height was taken as $\Delta E_c=0.5eV$; the low field mobility μ_0 was assumed a function of the local ionized impurity concentration ($\mu_0 \approx 10^4 cm^2/V{\cdot}s$ in the emitter).

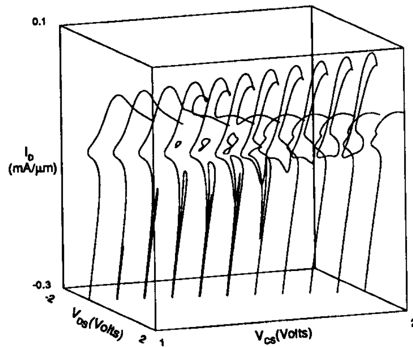

Figure 2:
CHINT I_D-V_{DS} characteristics for different V_{CS} ($L_{CH}=5\mu m$, $t_B=0.2\mu m$, $v_{sat}=1\times10^7 cm/s$) as obtained by predictor-corrector continuation. The emergence of loops, folds and disconnected branches are observed with increasing V_{CS} ($\Delta V_{CS}=0.1V$).

Close examination of the characteristics shows numerous topological transformations. Beginning as an accumulation mode FET at low V_{CS} (< 1.0V), the onset of RST initiates the formation of a slight NDR region in the $+V_{DS}$ direction ($\approx$ 1.0V). At higher V_{CS}, separate folds begin to appear for both V_{DS}>0 and V_{DS}<0 as illustrated in fig. 3 ($V_{CS}=1.21V$). To this point, the IV curves are still singly connected and in principle can be traced by one continuation simulation or more conveniently by two – in the $+V_{DS}$ and $-V_{DS}$ directions, both from $V_{DS}=0$.

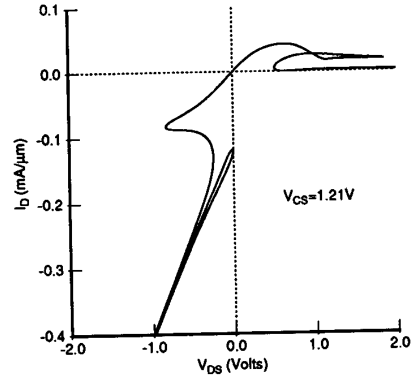

Figure 3:
CHINT I_D-V_{DS} characteristics for $V_{CS}=1.21V$ ($L_{CH}=5\mu m$, $t_B=0.2\mu m$, $v_{sat}=1\times10^7 cm/s$).

At slightly higher V_{CS}, a disconnected loop begins to appear in the left-hand plane, corresponding to a surface bounded by a minimum V_{CS} in the 3D space in fig. 2. As shown in fig. 4 ($V_{CS}=1.50V$), this closed loop and the needle-like fold emanating from the bottom of the left-hand plane both continue to open, and the "S-shaped" notch in the right-hand plane (the knee reached by tracing backwards from $V_{DS}=+\infty$) moves leftward as V_{CS} increases. Note the multiplicity of anomalous $V_{DS}=0$ states which exist as single symmetric solution states – i.e., $T_e(x,y)=T_e(-x,y)$ – or in pairs of asymmetric solutions which are reflective transforms of one another [12]. Continuation simulations from the origin as in fig. 3 can only pick up the outer, singly connected component of fig. 4 which contains symmetric, paired and unpaired asymmetric states. The disconnected loop is traced by continuation in V_{DS} initiated after reflecting the unpaired states; by continuing from these same states in V_{CS}, starting points are obtained for loops which do not cross the $V_{DS}=0$ axis ($1.25V \le V_{CS} \le 1.35V$).

Between $V_{DS}=1.50V$ and $V_{DS}=1.55V$, the characteristic transforms into a loop which includes the origin, and a singly connected component which is multivalued but has no folds or intersections with the loop (fig. 5). The transformation between figs. 4 and 5 includes several component breaks and joins; at least two of the intermediate states are singly connected. One continuation simulation starting at the origin produces the new loop; starting points for the disconnected branch can be obtained by continuation from lower V_{CS} (where the branch is still connected to the origin) or by performing separate transient

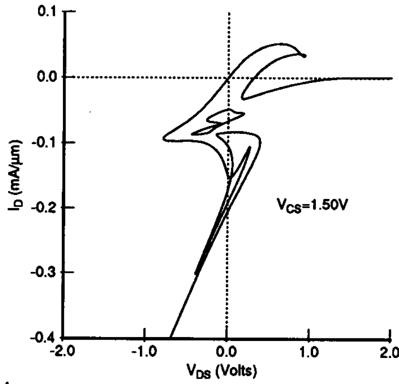

Figure 4:
CHINT I_D-V_{DS} characteristics for $V_{CS}=1.50$V ($L_{CH}=5\mu$m, $t_B=0.2\mu$m, $v_{sat}=1\times10^7$cm/s).

simulations – e.g. ramping V_{CS} quickly at $V_{DS}=0$ – as these points have been established as stable dc states [12].

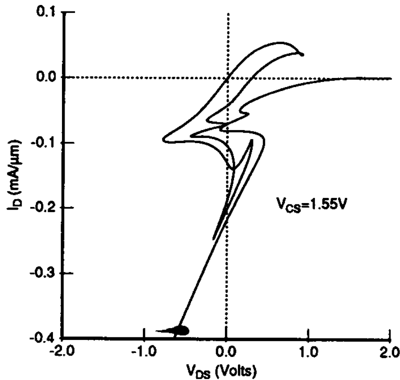

Figure 5:
CHINT I_D-V_{DS} characteristics for $V_{CS}=1.55$V ($L_{CH}=5\mu$m, $t_B=0.2\mu$m, $v_{sat}=1\times10^7$cm/s).

As V_{CS} is increased further, the *IV* characteristics maintain essentially the same topology, although the disjoint components separate further from one another. The lowest (stable) $V_{DS}=0$ state is forced to lower I_D (larger I_C), and the instability in the singly connected branch moves deeper into the right-hand plane.

Continuation in the pseudo-arclength produces a completely smooth evolution of the device state. In contrast, experimental measurements force abrupt transitions between states which are separated by finite distances in the (I,V) plane at limit points. These transitions force a global redistributions of state fields, corresponding to the formation or repositioning of high-field, high-temperature domains. Transient simulations of a typical measurement sequence eventually lead to the transition **k**→**u** as V_{DS} is increased from 0 as shown in fig. 6 ($V_{CS}=2.00$V). The resultant negative I_D at **u**, which has been observed experimentally [12], arises as the potential in the hot electron domains is lower than the drain due to carrier depletion. Note also that the lower *IV* branch in figs. 5 and 6 is no longer connected to the origin as in figs. 3 and 4, and therefore a reverse trace in V_{DS} from **u** after the state transition allows observation of the anomalous high-current $V_{DS}=0$ state, labeled **d**.

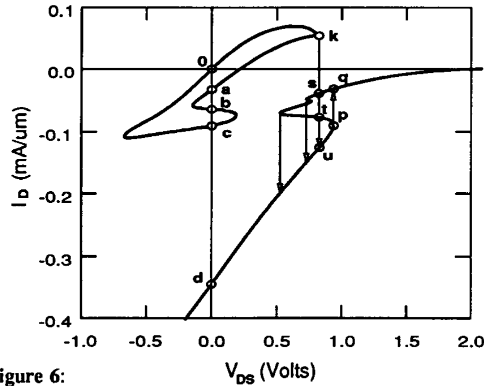

Figure 6:
CHINT I_D-V_{DS} characteristics for $V_{CS}=2.00$V ($L_{CH}=5\mu$m, $t_B=0.2\mu$m, $v_{sat}=1\times10^7$cm/s). Arrows indicate state transitions that occur via transient ΔV steps.

Maps of I_C-V_{DS} also show several interesting features. With I_D-V_{DS} plots, they completely define the device state since $I_C=I_S+I_D$. Fig. 7 is the characteristic for $V_{CS}=1.55$V; a loop and singly connected branch are visible. Although slices of I_C-V_{DS} space for a given V_{CS} are not symmetric, there is symmetry in the 3D space defined by $I_C(-V_{DS}, V_{CS}-V_{DS})=I_C(V_{DS}, V_{CS})$. Points defined by a single intersection with the $V_{DS}=0$ axis correspond to single symmetric states ($I_C=2I_D=2I_S$); points defined by two coincident intersections denote reflective, asymmetric pairs.

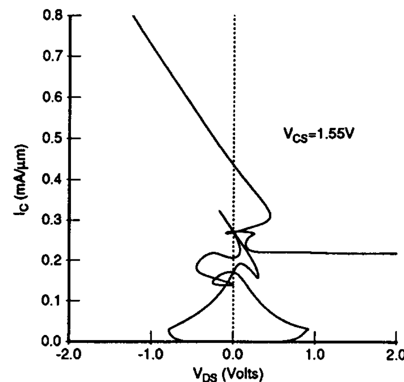

Figure 7:
CHINT I_C-V_{DS} characteristics for $V_{CS}=1.55$V ($L_{CH}=5\mu$m, $t_B=0.2\mu$m, $v_{sat}=1\times10^7$cm/s).

The positions of limit points and axes crossings are related directly to the physical properties which affect the formation of hot carrier domains. Fig. 8 shows the results of continuation simulations started from the origin for $V_{DS}>0$, using a higher saturation velocity v_{sat}. Both the V_{CS} and V_{DS} thresholds for causing bifurcations in *IV* increases with v_{sat}. Similarly the thresholds also increase for larger t_B and smaller L_{CH}. The critical ramp speed of a transient V_{CS} excitation required to induce the high-current $V_{DS}=0$ state **d** has similar dependencies which have been studied in quantitative detail in [13].

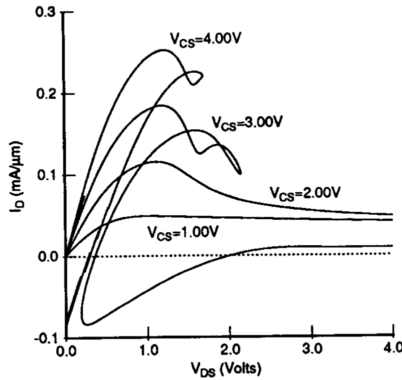

Figure 8:
CHINT I_D-V_{DS} characteristics for different V_{CS} ($L_{CH}=5\mu m$, $t_B=0.2\mu m$, $v_{sat}=2\times10^7 cm/s$) as obtained by predictor-corrector continuation. Results are shown only for the $V_{DS}>0$ branches initiated from the origin.

CONCLUSIONS

Multiply connected, self-intersecting *IV* curves are predicted for charge injection transistors using moment-based device simulation. The analysis suggests that the loops and folds in *IV* space, which cannot be continuously traced in measurements (or conventional simulations), are responsible for the nonlinear steps observed after the onset of real-space transfer (RST) in experiments. These results can qualitatively be reproduced by any transport model which incorporates RST self-consistently.

An essential feature of the analysis is the use of predictor-corrector continuation methods which allow the inspection of the full device phase space. In addition to providing global information about complex switching transitions, these mappings give reliable dc *stability* bounds, subsequently supported by more costly transient simulations. The understanding gained is invaluable in the application of RST transistors to the design of high performance systems.

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