Evidence for a real-space transfer of hot holes in strained GeSi/Si heterostructures

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A negative differential resistance is observed in *p*-type $Ge_{0.2}Si_{0.8}$ strained layers grown by molecular beam epitaxy on a Si (100) substrate. The peak to valley ratio is nearly 2 at $T = 77$ K. This effect is accompanied by an increase of the hole current into the Si substrate.

The effect of a negative differential resistance (NDR) due to the real-space transfer (RST) of hot electrons in multilayered heterostructures was theoretically predicted by Gribnikov[1] and Hess *et al.*[2] The first observation of such an effect was reported in modulation-doped GaAs/AlGaAs heterostructures.[3] Subsequently, the idea of a RST between heterostructure layers has been used to implement a three-terminal device, called the negative resistance field-effect transistor (NERFET), or charge-injection transistor (CHINT).[4-7] This device contains two conducting layers, separated by a potential barrier and contacted independently. One of these layers, referred to as the channel, has two surface contacts, source and drain. Application of a source to drain bias leads to a heating of channel electrons and charge injection into the second conducting layer. The channel acts as a hot-electron *emitter* and the second conducting layer as a *collector*. The device shows a strong negative differential resistance (NDR) in the source-drain characteristic (the NERFET action) and an efficient control of the injection current by the drain voltage (the CHINT action). Since the early reports, the CHINT/NERFET device has been extensively studied, both experimentally[8-11] and theoretically.[12,13] All the experiments reported so far have dealt with III-V compound semiconductor heterostructures and the RST of conduction-band electrons.

This letter describes the first observation of a RST of holes in strained-layer heterostructures of $Ge_{0.2}Si_{0.8}$/Si. Besides offering potential applications of NERFET/CHINT devices in silicon circuits, this system is attractive for studying the physics of hot holes. Its properties are different from those implemented in III-V compound semiconductor heterostructures in a number of respects. Strain induced by the lattice mismatch between the $Ge_{0.2}Si_{0.8}$ layer and the Si substrate splits the light and heavy hole bands of $Ge_{0.2}Si_{0.8}$ around the Γ point. Most of the band-gap discontinuity at the $Ge_{0.2}Si_{0.8}$/Si interface falls in the valence band; the potential barrier for holes in $Ge_{0.2}Si_{0.8}$ entering Si is around 0.17 eV.[14,15] Unlike electrons in a $GaAs/Al_xGa_{1-x}As$ system, hot holes participating in the RST across the $Ge_{0.2}Si_{0.8}$/Si interface are not subject to an intervalley scattering which may slow down the RST process.[13]

Our device structure is illustrated in Fig. 1. The sample was grown by molecular beam epitaxy (MBE) at 550 °C on a Si (100) substrate. The substrate was chosen to be *n* type, doped by As ($N_D = 2\times10^{18}/cm^3$). The first epitaxially grown layer was a 1000-Å-thick *p*-type Si collector layer with a boron concentration of $N_A = 10^{18}/cm^3$. The next one was a barrier formed by 2000 Å of Si doped with As ($N_D = 1.4\times10^{16}/cm^3$), and finally, a layer of 500-Å-thick pseudomorphic $Ge_{0.2}Si_{0.8}$ (boron doped, $N_A = 4\times10^{17}/cm^3$), forming a channel followed by a 200-Å-thick intrinsic Si cap layer. Details of the MBE growth of such $Ge_{0.2}Si_{0.8}$/Si structures have been described previously.[16]

The device area was defined by a 1200-Å-deep mesa etch performed in CF_4/O_2 plasma. Subsequently, 3000 Å of plasma oxide was deposited at 200 °C for isolation between devices and to serve as an implantation mask as well. The oxide was patterned and etched to define the source and drain regions and implantation of BF_2 at energy 30 keV and dose $1\times10^{14}/cm^2$ was performed. Standard moments calculation gives a simulated implantation depth of ~ 1000 Å at this energy. Implanted B impurities were activated by a rapid thermal anneal at 850 °C for 10 s. The source to drain separation was 3 μm. Finally, 3000-Å-thick aluminum layers were deposited on the front and the back sides of the wafer and patterned to form contacts to the source, the drain, and the substrate. The device structure and corresponding band diagram in equilibrium and at a negative substrate bias are shown in Fig. 1.

Current-voltage (*I-V*) characteristics were measured with a Hewlett–Packard 4145B semiconductor parameter analyzer and a Tektronix type 576 curve tracer. Figure 2 shows the drain (I_D) and the substrate (I_{SUB}) currents plotted versus drain voltage V_D at different substrate biases V_{SUB}. The measurements were performed both at room and liquid-nitrogen temperatures. At low V_D, the drain current is governed by the channel resistance but is also affected by a series resistance of the source and drain contacts to the $Ge_{0.2}Si_{0.8}$ channel layer. At higher V_D, especially at $T = 77$ K, one clearly observes an onset of NDR in the source-drain characteristic, accompanied by a swing of the I_{SUB} in the direction corresponding to the injection of positive charge into the substrate. Such a swing is not observed in a measurement of I_{SUB} as a function of the source-to-substrate voltage without a heating voltage V_D applied between the source and the drain. This indicates that both features, the NDR in source-drain characteristic and the swing in the substrate current, result from an injection of holes into the substrate—the RST of $Ge_{0.2}Si_{0.8}$ holes. The onset of NDR occurs at relatively high drain voltages, and the injection of Ge_xSi_{1-x} holes into the Si

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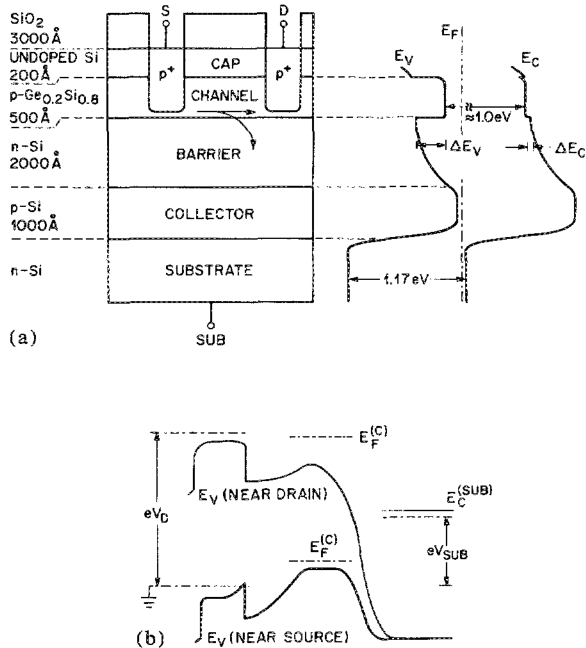

FIG. 1. Illustration of the Ge_xSi_{1-x}/Si NERFET device structure studied in this work. (a) Structure cross section and the equilibrium band diagram. (b) Valence-band diagrams in cross sections near the source and near the drain at negative substrate and drain biases, $|V_D| > V|_{SUB}|$. Quasi-Fermi levels are shown by broken lines. Most of the voltage difference $V_D - V_{SUB}$ drops across the *pn* junction between the collector layer and the substrate, and at high V_D the collector layer is depleted near the drain.

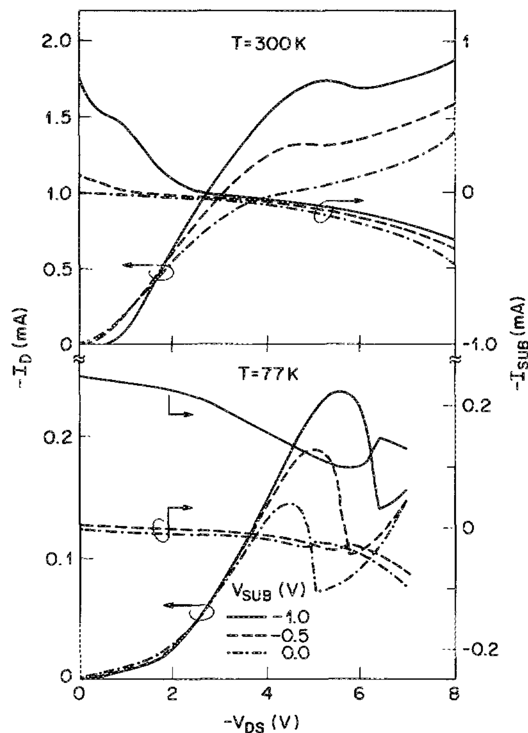

FIG. 2. Drain and substrate currents vs the drain voltage at substrate biases of 0, − 0.5, and − 1 V and temperatures $T = 77$ and 300 K. The NDR in source-drain characteristics is accompanied by a swing in the substrate current indicating an injection of holes into the substrate.

substrate is observed within a narrow range of V_D. The drop in I_D is not fully compensated by the upswing in I_{SUB}, indicating that the source current drops also. Such an effect has been seen before in CHINT/NERFET devices;[6] it is usually associated with a reconfiguration of the electric field in the channel at the onset of NDR.

For a qualitative understanding of the observed characteristics let us first discuss the potential of the floating collector layer. As seen from the diagram in Fig. 1(b), a negative voltage applied to the substrate results in a forward bias of the collector-to-substrate *pn* junction. Application of a negative voltage to the drain makes the barrier-collector heterojunction forward biased, while the collector-substrate *pn* junction near the drain becomes reverse biased. The potential along the collector layer is not necessarily uniform even though the current along this layer may be negligible. This happens because part of the collector layer near the drain becomes depleted of holes and most of the lateral collector voltage drops along that region. At higher V_D, the collector is negatively biased with respect to the source and acts as a buried gate, controlled by the drain. Hence, an increase in V_D results not only in a larger current in the channel but also in a more negative potential of the collector, which leads to a reverse bias of the collector-substrate *pn* junction.

Under such conditions, holes injected into the collector layer by a RST process cannot proceed to the substrate contact. Instead, the RST flux results in a carrier accumulation in the collector, which raises its potential. The positive charge buildup in the collector depletes the channel and causes a NDR in the source-drain characteristic. The rise in the collector potential results also in an injection of "cold" holes from the collector to the channel, which at first stabilizes and then terminates the NDR in the source-drain characteristic. As the collector potential rises due to the injected holes, the collector-substrate *pn* junction near the source becomes forward biased, allowing for a current flow to the substrate, as can be observed in Fig. 2. The magnitude of RST current at a given bias configuration, and the question whether it leads to a NDR in the channel characteristic, depends on the intrinsic efficiency of the heating of holes by the lateral electric field and the potential barrier height.

It should be noted that in order to observe an efficient RST in any CHINT/NERFET devices (including the conventional ones where the collector is contacted directly), it is important that in the region of the channel where carriers are sufficiently hot to overcome the band-edge discontinuity, the electric field in the barrier layer be directed so as to aid the drift of injected holes through that layer. Otherwise most of the carriers slide back to the channel. Thus, observation of the RST requires the existence of a range of drain voltages in which the channel electrons are hot enough at channel points *prior to field reversal.* This requirement we found particularly difficult to fulfill in samples with a structure as shown in Fig. 2 but grown on a *p*-type substrate. Those samples did not show any NDR, since application of the negative voltage to the drain caused substantial leakage current of holes from the collector to the drain, before the RST of the channel holes

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could develop in the opposite direction. As is clear from the band diagram in Fig. 1, our choice of an n-type substrate helps to preserve the desired direction of the electric field across the barrier region, even when the drain is negatively biased with respect to the substrate. Most of this bias drops across the reverse biased p-n junction formed between the collector layer and the substrate.

In conclusion, we have demonstrated a negative differential resistance in a p-doped $Ge_{0.2}Si_{0.8}$ channel of a GeSi/Si NERFET. Our results represent experimental evidence of the real-space transfer of hot holes across the valence-band discontinuity in this technologically important heterostructure. The measured peak to valley ratio was nearly 2 at 77 K. Several modifications in the device structure are required to increase this ratio and to observe a pronounced CHINT action. The channel length should be reduced in order to achieve the high electron temperature, required for an RST, at much lower V_D. For the same reason, the source and drain contact resistances have to be substantially improved. Finally, it would be advantageous to replace the p^+-Si collector layer by a p^+-Ge_xSi_{1-x} layer in order to limit the leakage current at high drain voltages by a band discontinuity between the barrier and the collector layer.

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