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ABSTRACT

We have reviewed the current status of silicon heteroepitaxy — a technique capable of growing single-crystal semiconductors, such as Ge or GaAs, on silicon substrates. Based on our assessment, growth of device-quality heteroepitaxial materials is possible and within reach. We predict that this technique will become dominant in the microelectronics of 1990s. The future hybrid material systems will allow for the combination of high-speed III-V devices with silicon VLSI in the form of a monolithic chip on a low-cost silicon substrate. Moreover, the union of germanium, tin, and III-V compound semiconductors with silicon will create a new range of possibilities for optoelectronic systems. We recommend an immediate organizational action to ensure our company the role of leadership in this emerging technology.

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TECHNICAL MEMORANDUM

1. Introduction

In the past few years the selectively doped GaAs/AlGaAs heterojunction transistor (also known as HEMT, or the high electron mobility transistor) has emerged as a serious contender for very high speed logic circuits. To wit, in 1983 Rockwell International reported [1] a switching speed of 12.2 ps with 13.6 fJ/stage power-delay product in a 1-μm gate HEMT ring oscillator at 300 K. The speed advantage of HEMT results mainly from its higher saturation velocity of electrons (2×10^7 cm/s at 300 K and 3×10^7 cm/s at 77 K, see [2]) and the lower source resistance (Rockwell devices [1] had $R_s \approx 0.5\ \Omega \cdot$ mm). The high electron mobility itself is not an important factor, since it takes place only at low electric fields ($\lesssim$ 10 V/cm), while at fields of order of 200 V/cm the drift velocity is already nearly saturated [2].

At the 1984 International Conference on Superlattices, Microstructures and Microdevices, a group from Fujitsu [3] described the status and trends of their HEMT technology aimed at integrated circuits. Particularly impressive was their achieved control of the threshold voltage: 19 mV standard deviation over a 2" wafer with 0.5 μm-gate HEMT's.

It has been argued for several years that GaAs devices such as HEMT may have an edge in

small-signal and logic front-end applications. With the above mentioned recently achieved threshold control it is now argued that HEMT will become a leader in large-scale integrated circuits. Here one talks not only about large digital systems ("supercomputers") at liquid nitrogen temperatures, but also about the VLSI which so far has been a sovereign domain of silicon technology. The main obstacle (hoped to be overcome) quoted by the proponents of HEMT is the lower quality of GaAs epitaxial layers (typically 200 - 300 fatal defects per cm^2, as contrasted with silicon's 0.1–0.05).

In our view, a more fundamental handicap of HEMT (or any other device grown on bulk III-V compound substrates) is the *cost* of the material. As will be discussed in Section 2, cost consideration will probably exclude bulk GaAs or InP substrates from VLSI applications. This conclusion is shared by a majority in the semiconductor industry. Most of the experts foresee a separation of markets between Si and III-V compounds — with different mature technologies catering to distinct requirements. In this view, the entire VLSI market will remain held by silicon, while the III-V compounds will be used at lower integration levels whenever the Si technology cannot do the job — that is in very high speed, and, especially, in optoelectronic applications.

We see a different perspective. In our opinion, the winning technology will be the one that can *combine* the low cost of silicon with the often superior and more versatile properties of III-V materials. Such a combination can be provided by a heteroepitaxial growth of single-crystal III-V compound layers on Si substrates. A number of recent experimental results give us grounds to believe in the fundamental soundness of this approach. These results, reviewed in Section 3, allow us to state resolutely that the fabrication of high-quality III-V compound layers on silicon is possible and within reach. A closely related development is the heteroepitaxial growth of other Column IV elements (Ge, Sn) on silicon substrates. Layers of germanium, tin, and their alloys can serve as intermediate layers facilitating the subsequent growth of III-V compounds (as will be discussed in Section 4), but also have various direct (e.g., photovoltaic) applications themselves. In the latter regard we should mention the recently proposed and fabricated germanium infrared detector on a silicon chip [4]. This single-crystal Ge/Si structure (reviewed in Section 3) works as an efficient photodetector in the wavelength range of 1.3–1.5 μm (the range of optical-fiber communications)

and its manufacturing process is entirely compatible with the Si IC technology. Of great interest also is the $Sn_x\ Ge_{1-x}$ alloy (discussed in Section 4), which not only can provide a perfect lattice match to GaAs at $x = 0.85\%$, but also can be expected to possess a *direct gap* at $x \gtrsim 26\%$. Such a material will have an extremely high mobility and also will offer the possibility of fabricating LED's and even lasers using only Column IV elements.

These hybrid material systems will allow for the combination of high-speed GaAs devices (such as HEMT) with silicon VLSI in the form of a monolithic chip on a low-cost silicon substrate. Monolithic chips have a tremendous advantage in the cost of packaging over hybrid circuits composed of devices on separate chips. In most applications savings will be realized from the reduction in system's size, weight, power consumption, board costs, etc. Moreover, the advantage of hybrid material systems lies not only in the economics, but also in their potentially higher performance. For example, most of the parasitic impedances associated with interchip communication will be eliminated. In the longer run, diode lasers and LED's will form optical links for high-rate data transmission between different areas of the same chip as well as between different chips in a larger system. Moreover, the union of tin, germanium, and III-V compounds with silicon will create a new range of possibilities for optoelectronic systems.

In our view, such combinations will become standard in the semiconductor industry of 1990s. The main purpose of the present Memorandum is to argue convincingly this point of view. We stress that it calls for a radical revision of the directions in microelectronics. The new approach should emphasize the unity of Column IV and III-V semiconductors in the future device structures, rather than a coexistence of widely divergent technologies aimed at different applications. Conclusions will be summarized in Section 5, where we shall outline what we see as the first necessary step in this direction, describe the scope of the effort required, and the necessary special equipment.

2. *Cost Comparison of Si and GaAs Wafers*

At present, high-speed integrated circuits using MESFET's or HEMT's are fabricated on bulk

compound-semiconductor wafers. This approach is not cost effective. For example, a 100-mm polished GaAs wafer costs about $400 which is over 25 times that of a corresponding Si wafer (see Table 1).

As the GaAs crystal-growth and wafer-shaping operations move down the learning curve, the cost of GaAs wafers will decrease. However, the cost of a bulk GaAs wafer will never become comparable to that of Si. This is because:

1. Higher raw material cost: High-purity raw material of GaAs costs about $700/kg which is about 13 times most expensive than Si. This is due to the high costs of mining and purifying gallium and arsenic, both are scarce in the earth's crust, while Si comprises 25% of the earth's crust and is second only to oxygen in abundance.

2. Fragile material: Since GaAs is a softer and more fragile material than Si, greater care must be exercised in GaAs wafer preparation. This results in substantially higher cost of wafer-shaping operations.

3. Higher density: GaAs has higher density (5.32 g/cm^3 as compared to 2.33 g/cm^3 for Si) and for a given diameter GaAs wafer must be thicker than Si to avoid breakage. The cost of GaAs raw material required for a wafer is 40 times more than that for a Si wafer.

4. High vapor pressure: Unlike Si, which has a relatively low vapor pressure at its melting point ($\sim 10^{-6}$ atm. at 1420°C), both gallium and arsenic have much higher vapor pressures at the melting point of GaAs (10^{-4} and 1 atm. respectively at 1238°C). To prevent decomposition of the melt during crystal growth, one has to make elaborate modification of the conventional Czochralski process (e.g., using a liquid encapsulation method). This also contributes to the higher cost per unit volume of GaAs ingot.

Referring to the bottom row of Table 1, the wafer cost (not yet processed) per unit area is $0.63/$cm^2$ for Si and $17/$cm^2$ for GaAs. The cost of bulk GaAs wafers is expected to remain an order of magnitude higher than Si in the foreseeable future.

Therefore, in our view, a fundamental handicap of devices fabricated on bulk compound-semiconductor wafers is the *cost* of the material. It may appear that for a highly sophisticated chip almost any cost of the wafer can be justified by the added value of electronic circuitry. However, according to an empirical law [5], for every more sophisticated chip, the initially high price decreases as its production technology matures, and it eventually settles at a price which is unacceptably low for the use of III-V compound-semiconductor wafers. This law is illustrated in Fig. 1 for dynamic random-access-memories. As can be seen from the figure, the price of a packaged DRAM chip of any complexity drops over time to roughly the same level of less than $2.00 per chip. Compared to that level, the $17/cm^2 cost of GaAs wafers is prohibitively expensive. In our view, the cost consideration is likely to exclude from VLSI applications any ICs based on GaAs or InP bulk wafers.

From this conclusion (which is shared by most of the experts in microelectronics) one often draws a vision of the future semiconductor industry in which there is a separation of markets between Si and III-IV compounds with different technologies catering to distinctive requirements. We believe, however, that such a coexistence of separate technologies can only be a temporary solution which may only last for another five years or so. In the long run (say, 10 years) this approach is not cost effective and it will yield to the emerging technology of monolithic hybrid material systems on low-cost Si substrates. Economic and technical advantages of such systems are self-evident. Their practical feasibility has become apparent in light of the recent (mainly 1984) dramatic developments in the field of silicon heteroepitaxy. These developments will be reviewed in the next section.

3. Heteroepitaxial Growth on Silicon Substrates

The heteroepitaxial combination of silicon with other semiconductors is complicated by the lack of a suitable lattice-matched partner. A rule of thumb in heteroepitaxy has been that the growth of a good interface requires a lattice mismatch of less than 0.5%. This requirement in the case of silicon is satisfied only by gallium phosphide and aluminum phosphide (GaP and AlP have a

perfect lattice match to each other and an acceptable 0.37% mismatch to Si). Investigation of the Si/GaP system by MBE has been recently reported by a Dutch group [6]; its application in the optical pickup "lightpen" is being implemented by Philips Laboratories. A difficulty in creating a GaP/Si heterostructure is that GaP tends to decompose during growth into gallium and phosphorus and then dope silicon [6]. This problem does not arise in the case of Ge which is chemically compatible with Si, but their lattice mismatch is substantial (4%) with Ge having the larger lattice constant. The Ge/Si heterostructure is normally replete with misfit dislocations, which make it difficult to use the electronic properties of the interface. An important advance in this regard is afforded by the strained-layer epitaxy technique [7] which allows one to grow thin layers of $Ge_x Si_{1-x}$ alloy on a silicon substrate virtually free of dislocations (the larger alloy lattice compresses to be accommodated by the Si lattice). The maximum thickness of the strained layer (beyond which one has incommensurate growth with the strain relaxed through generating dislocations) depends on the alloy composition x and on the growth conditions. In the low temperature MBE growth of the strained layer the formation of dislocations is impeded by a kinetic barrier so that the actual dislocation-free strained-layer thickness can be an order of magnitude larger than that thermodynamically allowed under equilibrium conditions [7]. The strained layer can be capped by another Si layer which grows without distortion, and then the whole layer sequence can be repeated, forming what is known as the strained-layer-superlattice (SLS). The SLS of variously designed composition profiles can be grown by MBE virtually free of dislocations, providing silicon technology with the new materials of variable bandgap E_g and refractive index $\bar{n}$.

Speaking about heteroepitaxial materials one usually has in mind the utilization of their unique heterojunction properties: abrupt potential barriers, light wave-guiding, etc. The above-mentioned studies of silicon-based SLS and Si/GaP heterostructures are mainly directed toward the same goal. The goal we are stressing in this Memorandum is quite different in that we are not concerned with utilizing the interfacial properties of a heterojunction formed by silicon and another material. We are mainly interested in the possibility of growing high-quality layers of the desired material on a silicon substrate — with intermediate layers if necessary. An example of such an

approach is the Ge/Si photodetector [4], whose structure and the band diagram are shown schematically in Fig. 2. In this structure the operating region (Ge pin diode of active thickness d) is actually removed from the interface by a heavily doped buffer layer W. It turns out that the quality of the heteroepitaxial material in the operating region is substantially better than that near the interface, as is evidenced by the transmission electron micrograph presented in Ref. 3. Of the many defects introduced by the lattice mismatch only threading dislocations persist far from the interface, and even their density gradually drops down. The measured quantum efficiency of this detector in the wavelength range 1.3–1.5 μm was found to be identical to that of commercially available pure Ge detectors ($\approx$40%). Its manufacture is entirely compatible with the silicon IC technology. To implement a complete optoelectronic system (receiver for fiber optics communications), one needs a patterned growth of Ge detector structures in selected areas of a Si wafer, with the rest of the wafer containing the VLSI circuitry being protected during the growth by an insulator layer. Such a patterned MBE growth does not appear to present any additional difficulties and in the instance of Si on Si it has been successfully tried before [8].

Recently, there have been several reports of a successful growth and patterning of GaAs single-crystal layers on Si substrates [9-15]. Sheldon et al. [9] reported single-crystal GaAs layers grown on a Si substate with an intermediate Ge layer. The entire heterostructure was grown by MBE. The quality of GaAs is indicated by the measured mobility which was only 15% lower than that for GaAs homoepitaxially grown by MBE on a GaAs substrate. The observed photoluminescence signal at room temperature had an intensity of 50% of that for the MBE grown GaAs on GaAs. The authors [9] also demonstrated the feasibility of growing GaAs in selected areas of the silicon wafer by means of SiO_2 masking and lift-off patterning.

Choi et al. [10] reported GaAs MESFET's fabricated on Si substrates. In that work again the GaAs layers were grown by MBE on an intermediate Ge layer, but the latter was predeposited by e-beam evaporation. The fabricated devices showed good transistor characteristics. For a 2.1 μm — gate MESFET'S the measured transconductance was about 105 mS/mm. Very recently, the same group at Lincoln Laboratory reported [11] successful operation of an AlGaAs/GaAs double-

heterostructure laser fabricated by MBE on a Ge-coated silicon substrate.

In the past two years there were two reports of monolithic GaAs light-emitting diodes (LED) on a Ge-coated Si substrate [12,13]. Both works used metal organic chemical vapor deposition (MOCVD) of GaAs. The Japanese group [12] prepared the intermediate Ge layers by zone-melting recrystallization of amorphous Ge on SiO_2 - coated silicon wafers. In the Cornell work [13] the epitaxial germanium layers were vapor deposited prior to MOCVD.

The above results show convincingly that high-quality GaAs layers can indeed be grown on silicon substates. The use of intermediate Ge layers makes good sense since the lattice mismatch between GaAs and Ge is very small (0.13%), and since, on the other hand Ge grows well on Si. Nevertheless, new reports [14,15] have just appeared describing direct growth of GaAs and AlGaAs on silicon wafers — without germanium coating. These studies, done at Lincoln Lab [14] and IBM [15], employed molecular beam epitaxy.

Most of the remaining difficulties are associated with the large lattice mismatch between Si and Ge (4%) which generates dislocations in the epitaxial layer. These dislocations propagate in the subsequently grown epitaxial layer causing leakage between the active layers of the device [4,10]. We believe that this problem will be reduced or even eliminated in the future. The authors of [10] mentioned that the diode leakage current in their MESFET was considerably reduced when a thicker GaAs buffer layer was grown to lower the defect density in the active device layers. No such effect was observed in [4] when the thickness W of the buffer layer was varied from 0.3 μm to 1.25 μm. However, a significant lowering of the parasitic leakage was achieved by employing alternate grading schemes for the transitional $Ge_x\ Si_{1-x}$ alloy region. Various techniques are being currently explored with the purpose of further improving the quality of heteroepitaxial layers by blocking the propagation of misfit dislocations.

Very recently a real breakthrough in this regard was achieved by Bean and coworkers [16]. Employing a new MBE growth trick called the "glitch grading," this group was able to produce nearly perfect germanium layers on a Si substrate. The method is illustrated in Fig. 3. Figure 3a

shows the schematic cross-section of the structure superimposed with its transmission electron micrograph. The layer of glitch grading corresponds to the region in epitaxial Ge/Si alloy, where the Ge content is repeatedly lowered from 100% to 70% and then restored back to 100%. The thickness of each glitch is about 100 Å and the periodicity is about 600 Å. It turns out that the lateral strain generated by the glitches blocks most of the dislocations from propagating beyond the glitch region. This is seen very clearly in the TEM picture of Fig. 3b, which shows an epitaxial germanium layer virtually free of defects.

4. The Tin Dimension

A new technique proposed recently by Luryi [17] is capable of preparing a silicon substrate for subsequent dislocation-free growth of a variety of semiconductors having a lattice constant less than 5.96 Å. The technique requires a low temperature epitaxial growth, such as MBE, and consists of depositing tin-silicon alloys on Si substrates. With this technique one should, in principle, be able to prepare a dislocation-free $Sn_x\ Si_{1-x}$ alloy with any desired $x \leqslant 0.5$, i.e., with any lattice constant between 5.43 Å and 5.96 Å.

It is well known that unlike Ge/Si alloys which mix in any proportion, the Sn/Si alloys exhibit phase segregation when cooled from the melt. Because of this there are no bulk solid alloys of Sn and Si. The problem of phase segregation does not arise, however, in a low temperature epitaxy, for which one can expect a smooth growth of uniform $Sn_x\ Si_{1-x}$ alloys on appropriately lattice-matched substrates.

Most of the misfit dislocations due to the lattice mismatch can be stopped from propagating by the method suggested by Matthews and Blakesley [18] which was successfully used [19,20] to grow a defect-free GaAsP/GaP strained layer superlattice on a lattice-mismatched GaP substrate. The diagram in Fig. 4 illustrates this method as adapted to the case of Sn-Si alloys. The diagram illustrates the growth sequence required to produce a $Sn_{0.5}\ Si_{0.5}$ alloy on a Si substrate, but it can be modified to grow a structure which terminates with $Sn_x\ Si_{1-x}$ for any $x \lesssim 0.5$. According to the idea of [18], misfit dislocations introduced during growth of the graded layer $z_1 - z_2$ will be trapped

in the SLS region $z_3 - z_4$ so that the alloy in the region $z > z_4$ is dislocation-free. This idea is conceptually similar and actually predates the glitch-grading scheme described at the end of the preceding Section.

The resultant alloy can be used as a substrate for growing other epitaxial materials of same lattice constant. To appreciate the scope of the new possibilities, consider the plot in Fig. 5 which shows the range of lattice constants available in Sn_x Si_{1-x} alloys (assuming their linear interpolation). We see that GaAs and Ge lattices are accommodated by an alloy with $x \approx 0.2$ and that even InP falls within $x \leqslant 0.5$ range. We have indicated by arrows in Fig. 5 the lattice constants of selected semiconductors and the corresponding lattice-matched tin/silicon composition.

We have also indicated in Fig. 5 the position of a tin-germanium alloy $Sn_{0.27}Ge_{0.73}$ which is of considerable interest in its own right. It has been predicted [21] that the alloy Sn_x Ge_{1-x} has a *direct* bandgap for $x \gtrsim 0.26$. It should be remembered, of course, that like the Sn/Si alloy, tin/germanium does not exist in the equilibrium bulk form because of the phase segregation when the alloy is cooled from the melt. It can be expected, however, to grow epitaxially on the right substate. For $x \gtrsim 0.26$ the Sn/Ge alloy will have the conduction band minimum in the Γ valley ($k = 0$) and therefore one can expect a very high electron mobility and low effective mass. Even more significantly, this direct-gap material offers a unique possibility of fabricating long wavelength (2.5 μm) LED's and lasers using only Column IV elements. We conclude that the development of epitaxial (nonequilibrium) tin-silicon and tin-germanium alloys will add an important new dimension and tantalizing perspectives to the field of silicon heteroepitaxy.

5. *Discussion and Conclusion*

We have outlined the emerging new technology: heteroepitaxy on silicon wafers. Let us summarize the main objective in the development of this technology, as we see it, stressing the difference from the "traditional" heterojunction epitaxy. In the latter one is usually interested in utilizing the unique heterojunction properties, such as abrupt discontinuities in the electron potential energy, the refractive index, etc. In silicon heteroepitaxy, we believe, one should be concerned not

so much with such properties as with the possibility of growing high quality layers of a desired material (e.g., Ge or GaAs) on a silicon substrate — with whatever intermediate layers necessary to provide the material quality in the working layers. We have reviewed the recent work and concluded that this possibility is virtually proven, at least for Ge and GaAs. These hybrid material systems would allow for the combination of high-speed GaAs devices as well as optoelectronic systems with silicon VLSI in the form of a monolithic chip on a low-cost silicon substrate. In our view, such combinations will become standard in the integrated circuits of 1990s. This vision calls for the establishment of a radically new direction in microelectronics, marked by the *convergence* of silicon and compound-semiconductor technologies rather than their separate developments.

As far as we know, nowhere in the world today is there a base for such a concerted development. Within AT&T Bell Laboratories it would require a dedicated effort on the scale of one laboratory. One certainly would need a comprehensive MBE system, similar to one designed recently by Bean [22] but equipped with two interlocked growth chambers, so that it would be possible to switch between Si/Ge/Sn growth and GaAs/GaAlAs growth without breaking the vacuum. Such a system capable of handling 125 - 150 mm wafers with a reasonable throughput would cost about $2*M*. One would also need an MOCVD system ($200*K*) for heteroepitaxy of III-V compounds. A very important requirement is a processing facility (low-scale but state-of-the-art) which would be able to handle both silicon and gallium arsenide. It is essential that such a facility should have a fast turnaround (on the scale of a week).

It is time to convert the technology of silicon heteroepitaxy from the status of research of individuals into a large organizational effort. Investment today in such an effort will ensure a dominant role for AT&T in the microelectronics of 1990s.

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Table 1
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TABLE 1 — Cost Comparison of Bulk Si and GaAs Wafers

Semiconductor	Si	GaAs	Ratio of GaAs/Si
High Purity Raw Material Cost (M_1)	\$55/kg	\$700/kg	13
Volume per 100 -mm wafers§ (V)	4.32 cm^3	5.89 cm^3	1.36
Density (ρ)	2.33 g/cm^3	5.32 g/cm^3	2.28
Weight per 100 -mm wafer ($W = V\rho$)	10.07 g	31.33 g	3.11
Raw Material Cost per 100 -mm wafer (M_1W)	\$0.55	\$21.93	40
Cost of polished 100 -mm wafer (M_2)	\$15	\$400	27
Area of 100 -mm wafer (A)	78.54 cm^2	78.54 cm^2	1
Wafer cost per unit area (M_2/A)	\$0.19/cm^2	\$5.09/cm^2	27
Wafer cost per unit area for 30% yield ($M_2/A/0.3$)	\$0.63/cm^2	\$17/cm^2	27

§ Wafer thickness is 0.55 mm for Si and 0.75 mm for GaAs

References

[1] C.P. Lee, D.L. Miller, D. Hou, and R.J. Anderson, "Ultra High Speed Integrated Circuits Using GaAs/GaAlAs High Electron Mobility Transistors," *IEEE Trans. Electron Devices* **ED-30**, 1569 (1983).

[2] See the review by P.M. Solomon and H. Morkoc, "Modulation-Doped GaAs/AlGaAs Heterojunction Field-Effect transistors (MODFET's), Ultrahigh-Speed Device for Supercomputers," *IEEE Trans. Electron Devices* **ED-31**, 1015 (1984), and references therein.

[3] T. Mimura, K. Nishiuchi, M. Abe, and M. Kobayashi, "Status and Trends of High Electron Mobility Transistor Technology," *Proc. of the International Conference on Superlattices, Microstructures and Microdevices*, Champaign, IL., August 1984.

[4] S. Luryi, A. Kastalsky, and J.C. Bean, "New Infrared Detector on a Silicon Chip," *IEEE Trans. on Electron Devices*, **ED-31**, 1135 (1984); U.S. Patent "Long Wavelength Photodetector" filed in 1983 (patent item 9751-P).

[5] M.P. Lepselter, Private Communication.

[6] T. de Jong, W.A.S. Douma, J.F. van der Veen, and F.W. Saris, "Silicon Molecular Beam Epitaxy on Gallium Phosphide," *Appl. Phys. Lett.* **42**, 1037 (1983).

[7] See the review by J.C. Bean "Silicon MBE: from Strained-Layer Epitaxy to Device Application," preprint 1984, to be published in Journal of Crystal Growth (1985).

[8] J.C. Bean and G.A. Rozgonyi, "Patterned Silicon Molecular Beam Epitaxy with Submicron Lateral Resolution," *Appl. Phys. Lett.* **41**, 752 (1982).

[9] P. Sheldon, K.M. Jones, R.E. Hayes, B.-Y. Tsaur, and J.C.C. Fan, "Growth and Patterning of GaAs/Ge Single Crystal Layers on Si Substrates by Molecular Beam Epitaxy," *Appl. Phys. Lett.* **45**, 274 (1984).

[10] H.K. Choi, B.-Y. Tsaur, G.M. Metze, G.W. Turner, and J.C.C. Fan, "GaAs MESFET's Fabricated on Monolithic GaAs/Si Substrates," *IEEE Electron Device Lett.*, **EDL-5**, 207 (1984).

[11] H.K. Choi, T.H. Windhorn, B.-Y. Tsaur, G.M. Metze, G.W. Turner, and J.C.C. Fan, "GaAs MESFET's and AlGaAs Double-Heterostructure Diode Lasers Fabricated on Monolithic GaAsSi Substrates," *Proc. 42nd Annual Device Research Conference*, Santa Barbara, CA, July 18-20, 1984.

[12] Y. Shinoda, T. Nishioka, and Y. Ohmachi, "GaAs Light Emitting Diodes Fabricated on SiO_2/Si Wafers," *Jpn. J. Appl. Phys.* **22**, L450 (1983).

[13] R.M. Fletcher, D.K. Wagner, and J.M. Ballantyne, "GaAs Light-Emitting Diodes Fabricated on Ge-Coated Si Substrates," *Appl. Phys. Lett.* **44**, 967 (1984).

[14] B.-Y. Tsaur and G.M. Metze, "Molecular Beam Epitaxy of GaAs and AlGaAs on Si," *Appl. Phys. Lett.* **45**, 536 (1984).

[15] W.I. Wang, "Molecular Beam Epitaxial Growth and Material Properties of GaAs and AlGaAs on Si (100)," *Appl. Phys. Lett.* **44**, 1149 (1984).

[16] J.C. Bean, T.T. Sheng, A. Kastalsky, and S. Luryi, unpublished.

[17] S. Luryi, "A Method for Tailoring the Lattice Constant of Silicon Substrates for Molecular Beam Epitaxy," notebook entry November 10, 1983, Patent Item 10272-P.

[18] J.W. Matthews and A.E. Blakeslee, "Defects in Epitaxial Multilayers" in three parts: (1) "Misfit Dislocations," *J. Cryst. Growth* **27**, 118 (1974); (2) "Dislocation Pile-Ups, Threading Dislocations, Slip Lines and Cracks," *ibid.* **29**, 273 (1975); (3) "Preparation of Almost Perfect Multilayers," *ibid.* **32**, 265 (1976).

[19] G.C. Osbourn, R.M. Biefeld, and P.L. Gourley "A $GaAs_xP_{1-x}$/GaP Strained-Layer Superlattice," *Appl. Phys. Lett.* **41**, 172 (1982).

[20] J.E. Schirber, I.J. Fritz, L.R. Dawson, and G.C. Osbourn, "Quantum Oscillations in Strained-Layer Superlattices," *Phys. Rev.* **B28**, 2229 (1983).

[21] R.F. Kazarinov, notebook #61288, entry of March 8, 1983, unpublished.

[22] J.C. Bean, private communication.

Figure Captions

Fig. 1. Cost of silicon integrated circuits, illustrated in the instance of dynamical RAM chips, after Lepselter [5].

Fig. 2 Schematic diagram of Ge/Si single-crystal infrared detector [4].

Fig. 3 Single crystal Ge/Si structure with glitch grading.

a) Schematic diagram of the composition and a high magnification TEM of the structure.

b) Larger view TEM, showing dislocation blocking.

Fig. 4 Proposed growth sequence for producing defect-free $Sn_{0.5}$ $Si_{0.5}$ alloy [17]. The alloy is preceded by a strained-layer superlattice of *average* composition equal to that of the alloy. The superlattice period (which is of order 10^{-6}cm) is exaggerated in the picture. One or more glitch-graded regions can also be inserted in the sequence.

Fig. 5 Lattice constants of Sn_x Si_{1-x} alloys.

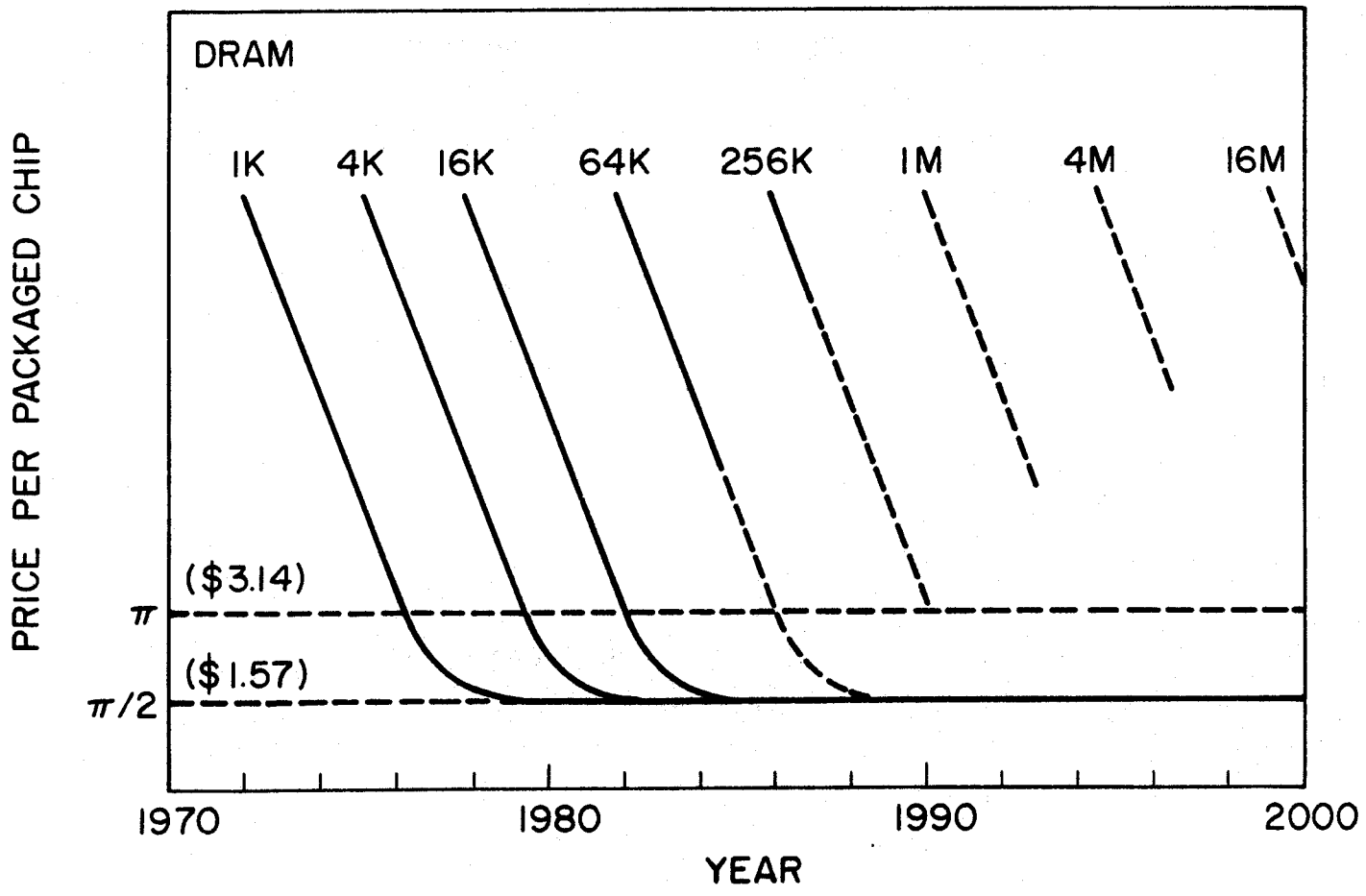
DRAM
1K
4K
16K
64K
256K
1M
4M
16M
($3.14)
π
($1.57)
π/2
1970
1980
1990
2000
YEAR
PRICE PER PACKAGED CHIP

FIG. 1

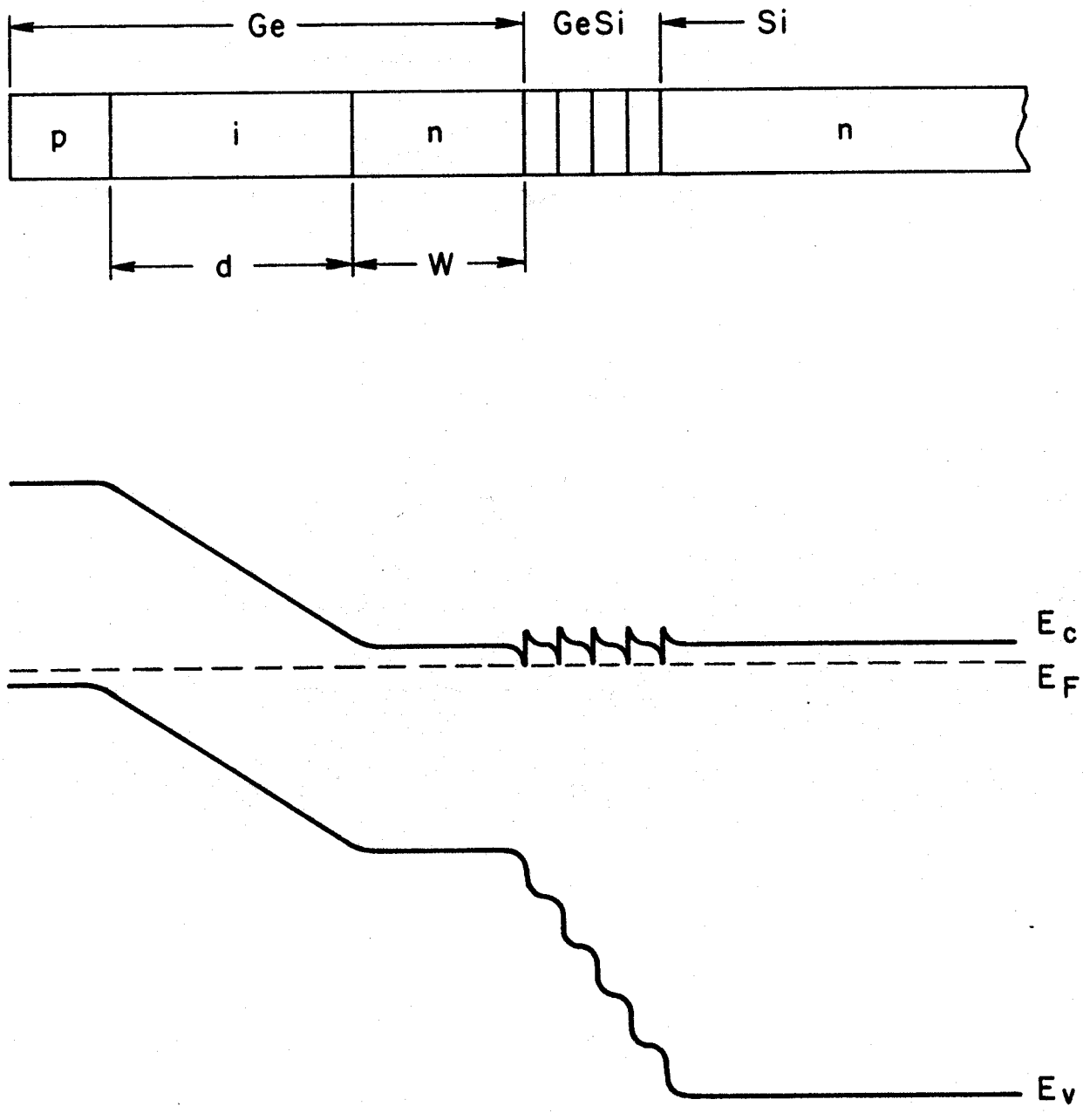

FIG. 2

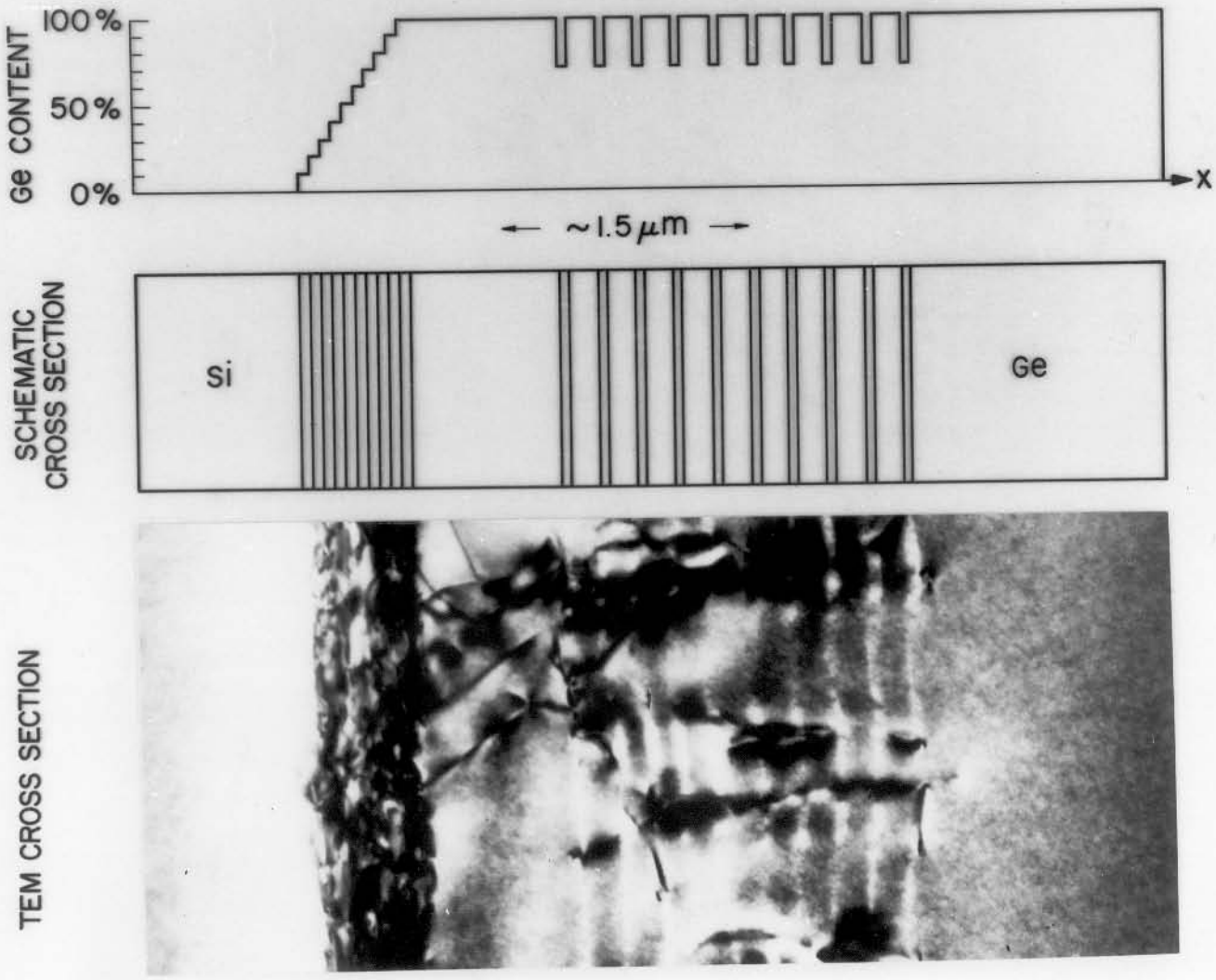
Ge CONTENT
100%
50%
0%
x
~1.5μm
SCHEMATIC CROSS SECTION
Si
Ge
TEM CROSS SECTION

Fig. 3a

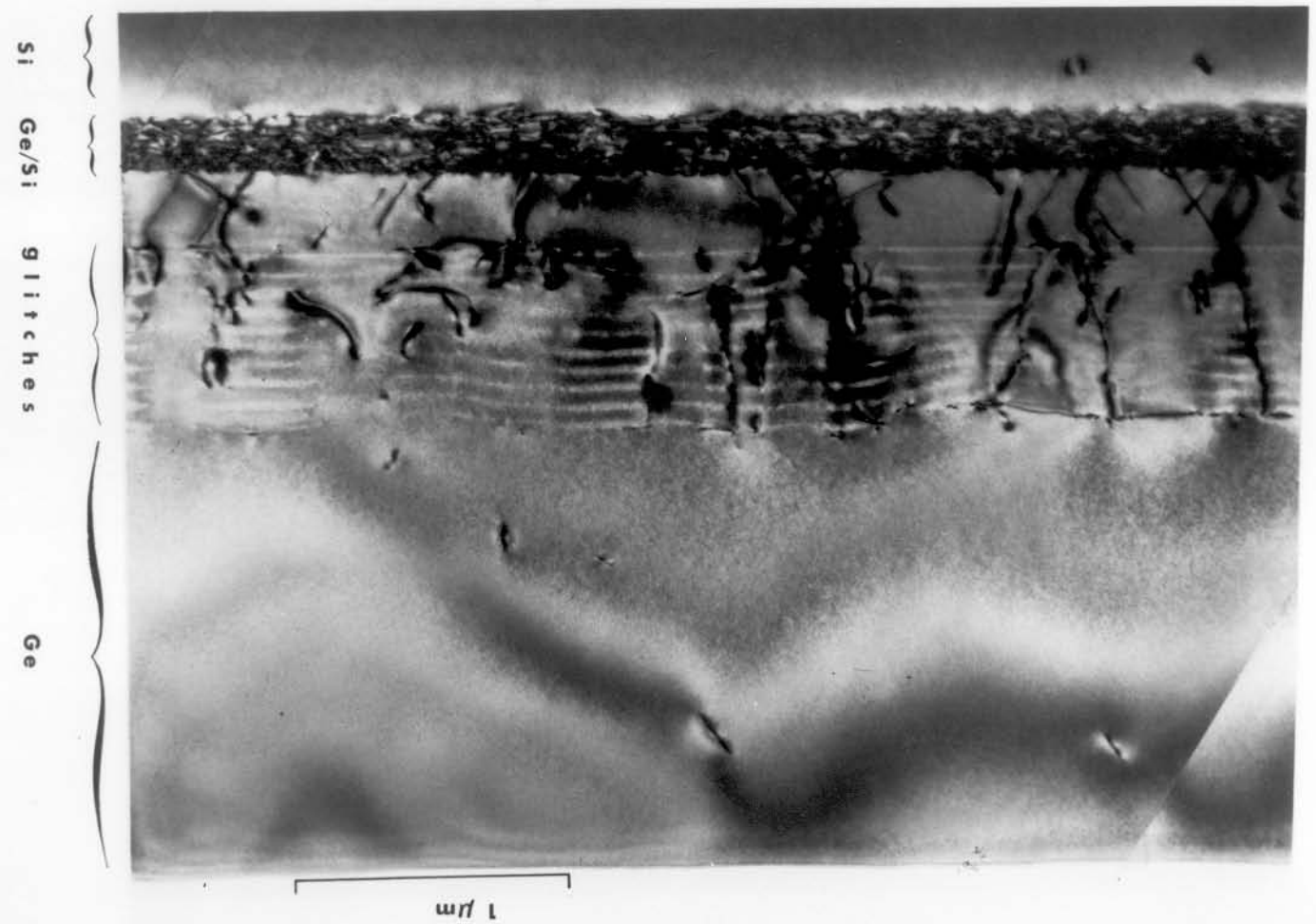

Fig. 3b

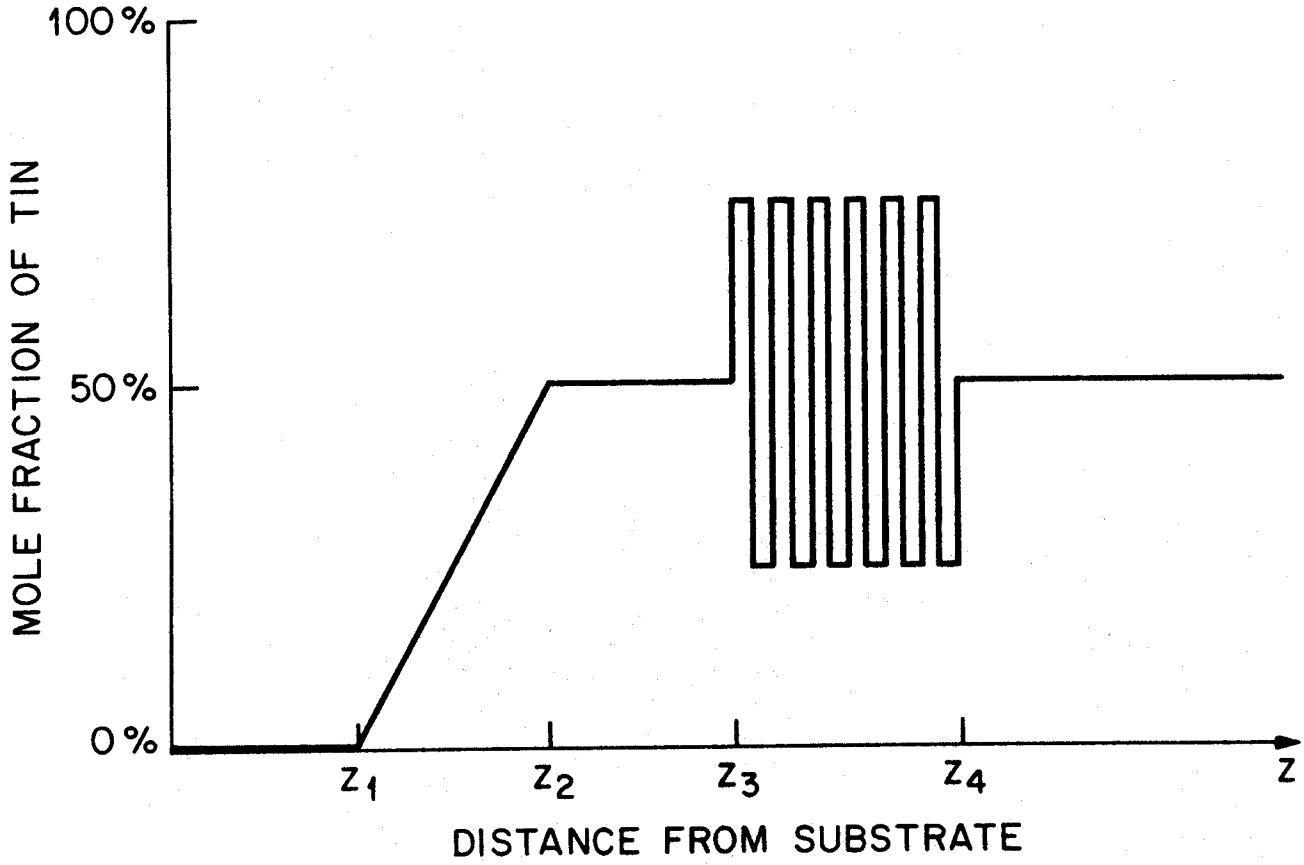
100%
50%
0%
MOLE FRACTION OF TIN
z_1
z_2
z_3
z_4
z
DISTANCE FROM SUBSTRATE

Fig. 4

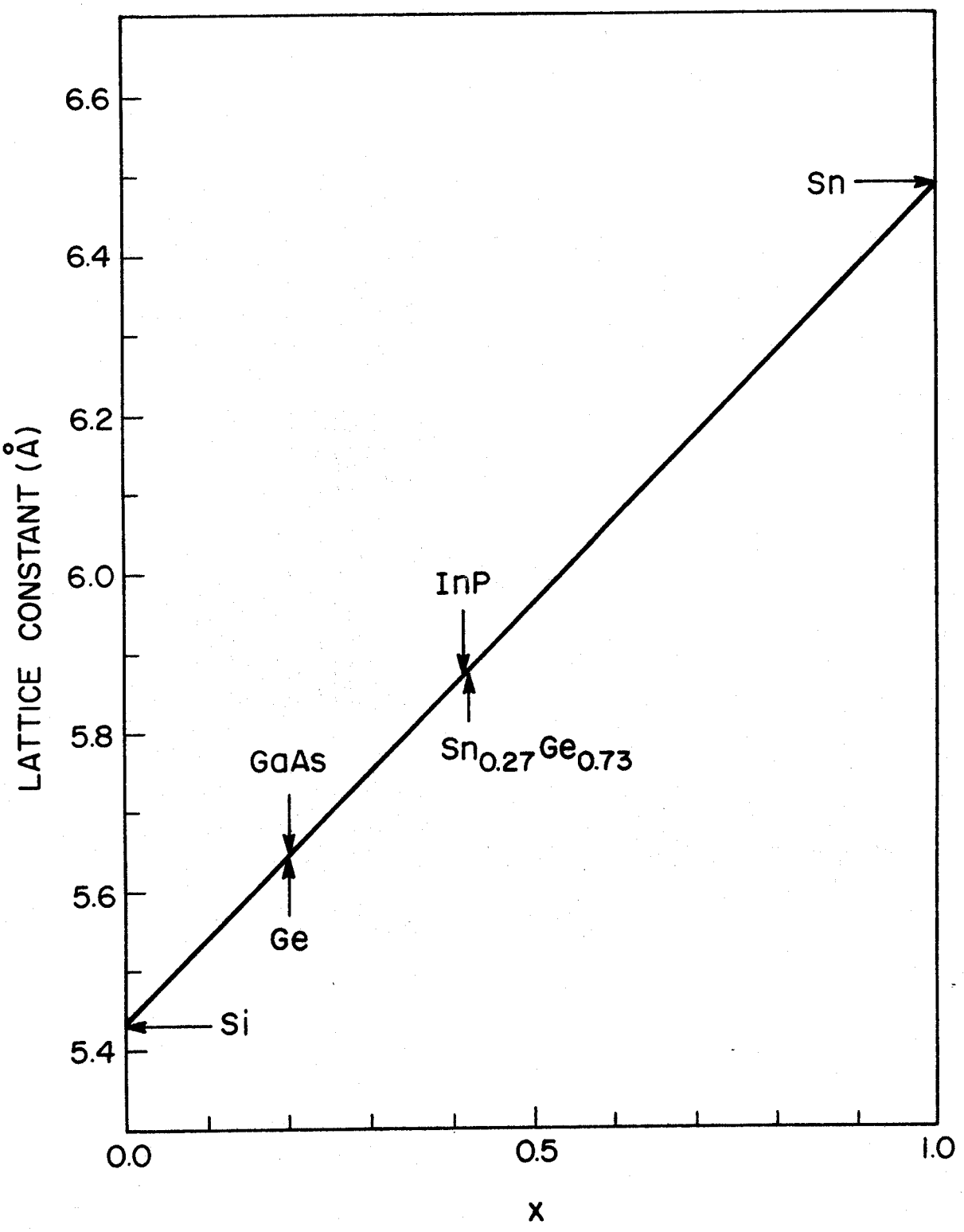
6.6
6.4
6.2
6.0
5.8
5.6
5.4
LATTICE CONSTANT (Å)
Sn
InP
$Sn_{0.27}Ge_{0.73}$
GaAs
Ge
Si
0.0
0.5
1.0
X

FIG. 6