Lab 5: Differential Amplifier.

1. OBJECTIVES

Explore the operation of differential FET amplifier with resistive and active loads:

Measure the common and differential mode open circuit voltage gains;

Measure the frequency response of gains and common mode rejection ratio.

2. INTRODUCTION

2.1. Differential pair.

In this lab we will study the basics of operation of differential amplifier. The heart of differential amplifier is differential pair composed of two transistors. In our case it will be two NMOS transistors (from ALD1105). We will bias both of these NFETs using NMOS current mirror like in previous labs (made of CD4007 NFETs). Figure 1 shows the circuit with no signal applied and no load connected.

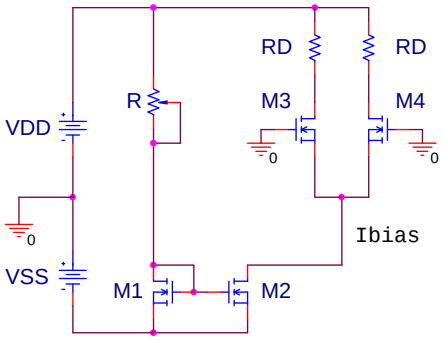

Figure 1.

In this circuit M3 and M4 NFETs are differential pair that is biased by M1-M2 current mirror. As long as M3 and M4 are identical and have identical R_D resistors in their drain circuits the differential pair branches are indistinguishable from each other and should each take ½ of I_{bias}. Hence M3 and M4 are biased by ½ of I_{bias} and should have corresponding (identical) gate transconductance and output resistance. Clearly, the task of biasing is almost exactly the same as in case of CS amplifier only now we need to have twice bigger I_{bias}.

Common mode operation is when input signal is applied to both gates of M3 and M4 simultaneously. Figure 2 shows this case. For the symmetric branches and ideal current source bias (I_{bias}) the M3 and M4 drain currents cannot be changed.

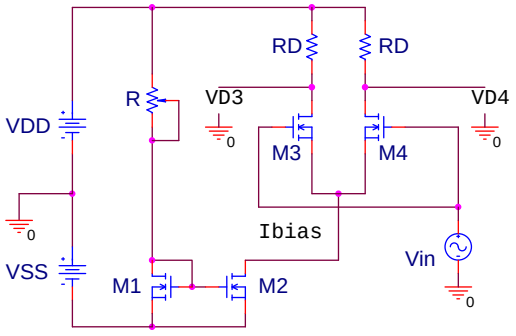

Figure 2.

Then no response to common mode excitation can be expected at either of branches (see operation of current source biased CS amplifier without any source bypass capacitor). In this ideal case drain signal voltages in both M3 and M4 branches are zero.

When the realistic current source bias is considered (M2 has finite output resistance) then some slight variation of the branch currents are possible and some signal can appear at drains of M3 and M4. Again, it is expected to be small like in case of CS amplifier without any source bypass capacitor. Clearly, for perfectly symmetric differential pair one can expect $V_{D3} = V_{D4}$. If the output is taken as a difference between drain voltages of M3 and M4 then the response to common mode excitation is going to be zero. In reality, there is always some mismatch between branches in differential pair and some difference between V_{D3} and V_{D4} can arise. The amount of output signal that appears in response to common mode excitation is characterized by **A_C – common mode voltage gain**:

$$A_C = \frac{V_{D3} - V_{D4}}{Vin} \to 0. \qquad (1)$$

Again, ideally A_C is zero and becomes nonzero only due to branch mismatch and finite output resistance of bias current source. Clearly, this logic is applicable to properly biased transistors, in our case we need to keep all transistors in saturation; hence there is always a limit on amplitude of input signal that can be tolerated.

Differential mode operation is when input signal is applied as a difference between gates of M3 and M4. Figure 3 circuit illustrates this case.

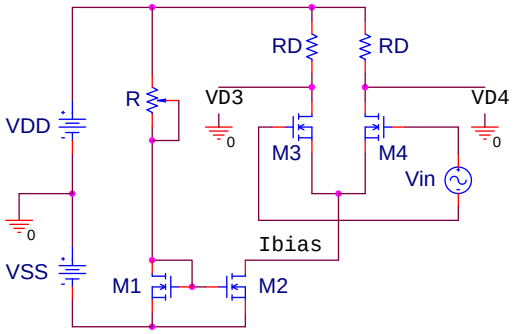

Figure 3.

Now the input signal changes gate voltages at M3 and M4 out-of-phase. We can visualize positive excitation as: ½ of it increasing V_{G4} above zero and ½ of it decreasing V_{G3} below zero. Hence, pure differential input corresponds to identical in amplitude but out-of-phase excitation of two branches of differential pair. Under input signal applied the drain currents in two branches change for the same amount but with different polarity. In example above, I_{D4} will increase above ½ I_{bias} and I_{D3} will decrease below ½ I_{bias} in response to positive half wave of differential input. Consequently, the V_{D4} will decrease below and V_{D3} will increase above their respective DC bias value (in ideal symmetric system these DC biases are the same, of course). Since sum of drain currents flowing through M3 and M4 should remain equal to I_{bias} (small difference can only arise due to finite output resistance of M2), the signal voltages at drains of M3 and M4 are equal in amplitude but out-of-phase. The amount of output signal that appears in response to differential mode excitation is characterized by

A_D – differential mode voltage gain:

$$A_D = \frac{V_{D3} - V_{D4}}{V_{in}} = g_m \cdot (R_D \parallel r_0). \qquad (2)$$

Common mode rejection ration is defined as:

$$CMRR = A_D / A_C \to \infty. \qquad (3)$$

2.2. Single ended output.

It is often desired to take output not differentially but from single end, i.e. from the drain of one of the branches with respect to ground. In that case the A_D would decrease twice ($A_D \approx \frac{g_m \cdot R_D}{2}$, r_0 is ignored) since only half of the input is being used to generate what is now called the output voltage. CMRR can degrade since the output resistance of M2 (r_{0M2}) matters in single ended output case. Common mode voltage gain becomes $A_C = -\frac{R_D}{2 \cdot r_{0M2}}$ and $CMRR = \left|\frac{A_D}{A_C}\right| = g_m \cdot r_{0M2}$.

Clearly, there is no need to have R_D in both branches of differential pair if only single ended output operation is expected. Namely, if the output is to be taken from drain of M4, then R_D in drain of M3 can be eliminated (Figure 4a).

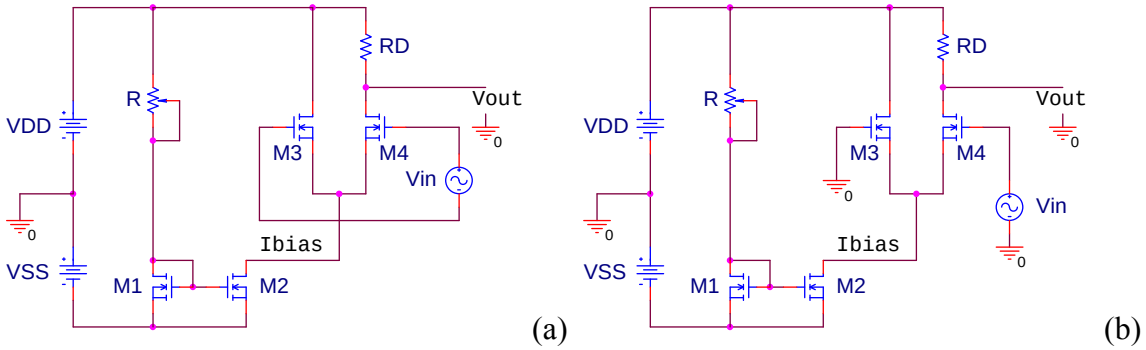

Figure 4.

If the input is also expected to be in single ended form one can ground the gate of one of transistors in differential pair, for instance, gate of M3. This type of connection is neither pure differential nor pure common mode but mix of these two.

Common mode part of input signal can be calculated as: $$V_{in}^{COM} = \frac{V_{G4} + V_{G3}}{2} = \frac{V_{in}}{2}, \quad (4)$$

and differential mode part of input signal is: $$V_{in}^{DIF} = V_{G4} - V_{G3} = V_{in}. \quad (5)$$

Now the expected single ended output voltage is:

$$V_{out} = A_D \cdot V_{in}^{DIF} + A_C \cdot V_{in}^{COM} \approx A_D \cdot V_{in} = -\frac{g_m \cdot (R_D \parallel r_0)}{2} \cdot V_{in}, \quad (6)$$

since A_C is often << A_D. It should be noted that it does not matter what gate is grounded. We could very well ground gate of M4 and apply signal to gate of M3 and would collect output voltage from drain of M4. Only sign of the gain would change (Equation 6). Clearly, the single ended gain of differential amplifier with "resistive load" is limited by the same considerations as in case of CS amplifier.

2.3. Active load.

Active load is expected to improve the differential mode voltage gain a lot. Figure 5 shows the schematic of the differential amplifier with active load. Firstly, the active load current mirror action will get rid of factor of two in denominator of equation 6, i.e. increasing gain twofold. Secondly, the R_D will be effectively replaced

with output resistance of an active load transistor, thus, gain will be increased further. Common mode voltage gain, on the other hand, will be reduced since for common mode operation the drain of M4 is effectively connected to ground through $1/g_{m5}$, where g_{m5} is gate transconductance of M5. However, whenever we have capacitive load (actual or parasitic one) the increased output impedance of the actively loaded differential pair would limit bandwidth of differential mode voltage gain. Parasitic capacitance in parallel with bias current source can degrade CMRR even before A_D starts to degrade. We will measure frequency response of differential amplifier with active load in lab. Active load will be constructed out of two PMOS transistors of ALD1105.

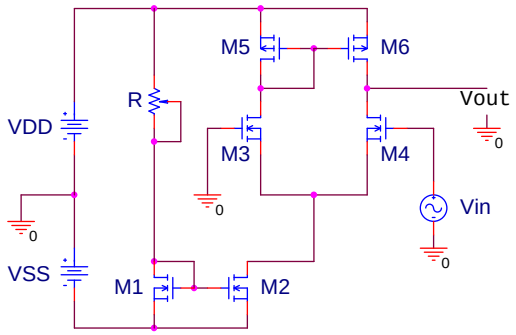

Figure 5.

With active load the voltage gain of the differential amplifier with single ended input will be:

$$A = \frac{V_{out}}{V_{in}} \approx A_D = -g_{mM4} \cdot \left(r_{0M4} \parallel r_{0M6}\right) \approx -g_{mM4} \cdot \frac{r_{0M4}}{2}. \qquad (7)$$

3. PRELIMINARY LAB

3.1. Consider circuit in Figure 1. Assume VSS = VDD = 5 V. Assume that M3 and M4 are both to be biased with 250 μA. Estimate the value of R that would lead to the desired bias. Use parameters of M1 and M2 from prelab of laboratory 1.

3.2. Consider circuit in Figure 2. Assume VSS = VDD = 5 V and R_D = 10 kΩ. Assume that M3 and M4 are both to be biased with 250 μA. Estimate the maximum amplitude of the input voltage that can be applied without driving FETs into nonsaturation?

3.3. Consider circuit in Figure 3. Assume VSS = VDD = 5 V and R_D = 10 kΩ. Assume that M3 and M4 are both to be biased with 250 μA. Use lab 2 experimental value of the gate transconductance for both M3 and M4. Calculate the differential mode voltage gains for differential and single ended outputs.

3.4. Consider circuit in Figure 4b. Assume all parameters from 3.3. Calculate the voltage gain defined as a ratio of Vout to Vin.

3.5. Consider circuit in Figure 5. Assume 250 μA biases for either of branches of differential pair. Estimate voltage gain (Vout / Vin) using your lab 2 data obtained for CS amplifier.

4. EXPERIMENT (*pay attention that 4.1 - 4.4 measurements are fast but 4.5 can take time*)

4.1. Assemble differential amplifier (Figure 1) using VDD = VSS = 5 V and R_D = 10 kΩ. Select 50 kΩ potentiometer and adjust it to obtain I_{bias} = 500 μA. Make sure that all transistors are in saturation.

Present the data confirming the saturation mode of M1-M4.

4.2. Perform measurements of the common mode voltage gain using circuit from Figure 2. Use sine wave input voltage with 1 kHz frequency. Adjust input voltage amplitude to produce enough output signal but with no distortions. Measure both the single end and the differential output A_C using oscilloscope.

Present the data in the form of table. Comment on results.

4.3. Perform measurements of the differential mode voltage gain on the same circuit. Apply input signal as shown in Figure 4b but keep R_D in both branches of differential pair. Measure both single end and differential output A_D using oscilloscope.

Present the data in the form of table. Comment on results. Calculate CMRR using 4.2 and 4.3 data.

4.4. Measure the differential mode voltage gain for the circuit in Figure 4b, i.e. remove R_D from M3 branch of circuit from 4.3.

Compare with 4.3 measurement results. Explain your observations.

4.5. Assemble circuit from Figure 5. Measure the differential mode voltage gain at 1 kHz. Adjust input signal amplitude to obtain undistorted output waveform (you might want to use voltage divider). Measure the corresponding common mode voltage gain. Measure high 3dB frequency of differential and common mode voltage gains and then for CMRR.

Present the data in the form of table. Compare with 4.4 measurement results. Explain your observations.

4. REPORT

The report should include the lab goals, short description of the work, the experimental and simulated data presented in plots, the data analysis and comparison followed by conclusions. Please follow the steps in the experimental part and clearly present all the results of measurements. Be creative; try to find something interesting to comment on.