A Low-Power, High-Linearity Filter Bank for Auditory Signal Processing Microsystem

Yingkan Lin and Milutin Stanaćević
Department of Electrical and Computer Engineering
Stony Brook University
Stony Brook, NY 11794–2350
Email: yingkan,milutin@ece.sunysb.edu

***Abstract*—We present an implementation of an auditory filter bank that decomposes the input signal into 16 parallel bands with central band frequencies ranging from 150 Hz to 10 kHz according to the mel-scale. The proposed integration of the designed filter bank in a microsystem for acoustic source separation poses a stringent constraints on the linearity and dynamic range of the filters. The capacitive attenuation is used to increase the voltage range at the input and the output of the filter. The simulation results demonstrate that the third order harmonic distortion of the bandpass filter with the central frequency of 150Hz is -59.6dB and dynamic range is 59.9dB. The power consumption of the filter bank implemented in 0.5μm CMOS technology is 36 μW.**

I. Introduction

Although the demand for the speech interfaces has recently significantly increased, the speech recognition can not achieve the satisfying recognition rates in the noisy environments leading to the need for advancement in the auditory signal processing [1]. Subband processing has been an important tool in the auditory signal processing of reverberant signals. There have been a wide range of analog auditory filter banks proposed in the literature mimicking the behavior of cochlea [2]–[4].

In the proposed acoustic separation system [5], [6], that interfaces the array of the miniature microphone arrays, we have demonstrated that the subband signal processing can improve the source separation performance in moderate reverberant environments. However, due to the linear mixing model in each filter bank, the requirements on the linearity in each subband, as well as the dynamic range, are high. Although, the gm-C filters can not achieve linearity that can be achieved by switched-capacitor filters, the choice of the gm-C filter implementation is dictated by the chip area and the power consumption requirements. The proposed filters also require large time constants leading to the design of operational transconductance amplifiers(OTAs) with very low transconductance. A 16 channel bandpass filter bank with center frequency from 150 Hz to 10 kHz is built in our system.

II. Low Transconductance High Dynamic Range OTA

A very low transconductance OTA can be achieved using a five transistor OTA implementation with the input transistors biased in the weak inversion region of operation. The OTA achieves very low power consumption and small area [7]. However, 1% harmonic distortion limits the input peak to peak voltage to less than 15mV. As a result, the dynamic range can not exceed -45dB which is insufficient in the proposed system. Another option is to used the bulk as the input terminal [8], but in this case the performance strongly varies between processes and runs. Applying the techniques of source degeneration, current division and cancellation in design of OTA, a few large time constant subthreshold gm-C filters are reported in the literature [9], [10] that achieve excellent performance in linearity and dynamic range.

The OTA structure used in the proposed filter bank is shown in Figure 1. The structure uses two methods to improve the linearity, source degeneration and current division. The transistor M_R is biased in the triode region and acts as the source degeneration resistor. Source degeneration improves the OTA linearity as M_R realizes the voltage to current conversion instead of the input transistor biased in the saturation region. To achieve the high resistance, M_R has to be a long channel transistor. The currents flowing into transistors M_1 and M_M are divided by factor M which is the ratio of their sizes. Considering that only the current of M_1 contributes to the output current, the effective transconductance of the OTA, G_m, is reduced by the factor of M+1 compared to the OTA implemented without the current division. Therefore, G_m can be calculated as:

$$G_m = \frac{i_o}{v_{id}} = \frac{g_{m_{M1}}}{1+(M+1)g_{m_{M1}}/g_{ds_{MR}}}, \quad (1)$$

where $g_{m_{M1}}$ is the transconductance of the input transistor M_1 and $g_{ds_{MR}}$ represents the small signal drain source conductance of M_R. We define the ratio of transconductances as

$$\alpha = \frac{(M+1)g_{m_{M1}}}{g_{ds_{MR}}}. \quad (2)$$

If α is much greater than 1, (1) can be further approximated as

$$G_m = \frac{i_o}{v_{id}} = \frac{g_{ds_{MR}}}{1+M}. \quad (3)$$

It is desirable to keep the α larger than 5. For a low power design, M_1, M_M and M_N operate in the moderate inversion. The moderate inversion operation leads to a high power efficiency compared to the strong inversion while it guarantees a larger input range than the weak inversion. In the filter bank

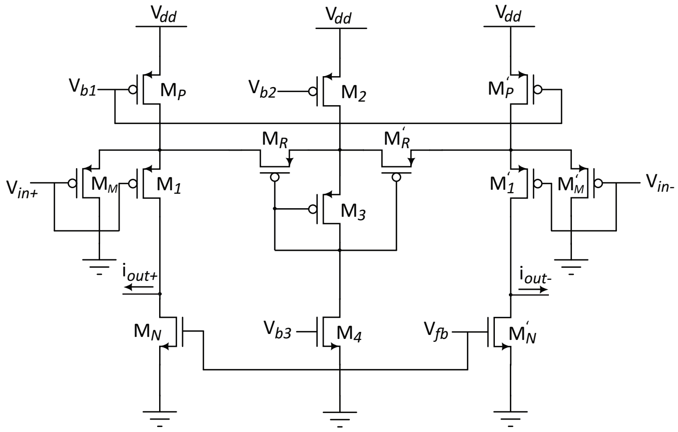

Fig. 1. Implementation of a low transconductance OTA.

design, the $g_{ds_{MR}}$ is adjusted by varying the V_{sg} voltage of M_R controlled by the current in the branch comprising M_2, M_3 and M_4.

The linearity of the OTA is mainly determined by the linearity of $g_{ds_{MR}}$, which is affected by the body effect. The third order harmonic distortion (HD_3) of the OTA can be calculated as [10]:

$$HD_3 \cong \frac{\gamma \cdot v_{SD}^2}{96(v_{SG} - V_{th})(2\phi_F - v_{SB})^{\frac{3}{2}}}, \tag{4}$$

where γ is the body effect constant, ϕ_F is the Fermi potential and v_{SD} represents the same potential change as the input signal. From (4), the harmonic distortion is mainly determined by $v_{SG} - V_{th}$:

$$v_{SG} - V_{th} = \frac{g_{ds_{MR}}}{\mu_p C_{OX} \frac{W}{L}} = \frac{(M+1)G_m}{\mu_p C_{OX} \frac{W}{L}} \tag{5}$$

In the design of the proposed filter bank, the smallest transconductance OTA is:

$$G_{mmin} = \frac{2\pi f_{cmin}}{C_{max}} \tag{6}$$

f_{cmin} is the lowest center frequency of the filter bank and C_{max} is the largest capacitor used. The lowest center frequency in our filter bank is 150 Hz, and due to area limitation, we choose C_{max} to be 10 pF. The requirement on the design of the OTA is that HD_3 is suppressed under -50 dB with 50 mV input amplitude. This means that the current division ratio, M, has to be greater than 10. The power consumption of the OTA increases linearly with M. Therefore, M is set to 10, which is the smallest value satisfying the linearity requirement and keeping the power consumption low at the same time.

The only constraint on g_m of transistor M_1 is to be 5 times bigger than the OTA transconductance. Therefore, when the G_m of OTA is varied in the filter bank, the bias current of M_1 and M_M, can be varied simultaneously to decrease the power consumption of OTA. The sizing of the transistors is shown in Table I.

TABLE I
TRANSISTOR SIZING IN THE OTA

M_1	4.8μ/4.8μ
M_M	48μ/4.8μ
M_P	6.3μ/6μ
M_N	8.4μ/27μ
M_R	1.5μ/108μ
M_2	6.3μ/6μ
M_3	1.5μ/90μ
M_4	4.5μ/3μ

A. *Noise Performance of OTA*

Due to the current division structure, the noise contributions of transistor M_M become negligible, as well as the contributions from M_P and M_R. Therefore, the output referred current noise density can be expressed as the sum of the noise contributions of M_1 and M_N. As the M_1 and M_N have the same biasing current, the total input referred white voltage noise of the OTA can be expressed as:

$$v_{in\_th}^2 = \frac{8kTng_m}{G_m^2} BW \tag{7}$$

where n is the subthreshold slope coefficient, k is the Boltzmann constant and T is the absolute temperature. g_m is the transconductance of M_1 and according to equation (3) can be expressed as:

$$g_m = \frac{g_{ds_{MR}} \times \alpha}{M} = \frac{\alpha(M+1)G_m}{M} \approx \alpha G_m \tag{8}$$

Therefore, the input white noise becomes:

$$v_{in\_th}^2 = \frac{8kTn\alpha}{G_m} BW \tag{9}$$

It can be observed that larger α guarantees less contribution of input transistor to the linearity of the OTA, at the cost of larger white noise. As a result, α is chosen to be 5 in order to trade off between linearity and white noise.

The input referred flicker noise can be computed as:

$$v_{in\_f}^2 \approx \frac{2}{C_{ox} G_m^2} \left(\frac{K_{Fp}}{W_1 L_1} + \frac{K_{Fn}}{W_n L_n}\right) \log(BW) \tag{10}$$

where C_{ox} is the gate oxide capacitance per unit area, W_1, L_1, W_n and L_n are respectively the width and the length of transistor M_1 and the width and the length of transistor M_N. The flicker noise coefficient K_{Fn} is few times higher than K_{Fp}, which leads to a bigger transistor area of M_N than M_1 in order to lower the 1/f noise.

III. SINGLE CHANNEL BANDPASS FILTER DESIGN

The dynamic range of gm-C filter is usually limited by the small linear input range of OTA. Capacitive attenuation can increase the linear range of the filter effectively [2]. A fully differential gm-C bandpass filter with capacitive attenuation is implemented using the designed OTA, with the single-ended implementation shown in Figure 2. The proposed implementation introduces additional OTA compared to the design reported in [11]. The voltage gain in the pass band, center

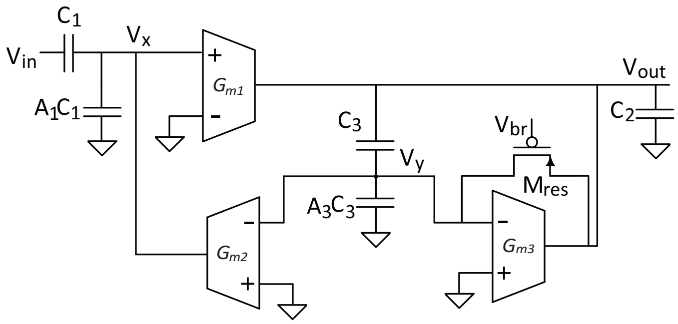

Fig. 2. Implementation of a single channel bandpass filter with capacitive attenuation.

frequency and quality factor of the proposed implementation are

$$A_v = \frac{(A_3+1)G_{m1}}{(A_1+1)G_{m3}} \tag{11}$$

$$\omega_o^2 = \frac{G_{m1}G_{m2}}{(A_1+1)C_1[(A_3+1)C_2+A_3C_3]} \tag{12}$$

$$Q^2 = \frac{(A_3+1)C_2+A_3C_3}{(A_1+1)C_1}\frac{G_{m1}G_{m2}}{G_{m3}^2}. \tag{13}$$

By choosing the proper ratio of the transconductances and attenuation ratios, the output voltage can have the same amplitude as the input voltage. Meanwhile, the input voltage of OTAs is attenuated by the capacitive attenuation. The transistor M_{res} functions as a large resistor which provides the DC bias path for OTA_2 and OTA_3.

High selectivity of the bandpass filter is required in the design of the source separation system. Therefore, Q is chosen to be 4 for the single channel filter with the voltage gain equals to 1. The input voltage range of all the OTAs in the filter has to be the same, so that no single OTA limits the harmonic distortion. This introduces additional constraint in the selection of the filter parameters. The input voltages of OTAs can be expressed as:

$$V_x = \frac{sV_{out}[(A_3+1)C_2+A_3C_3]+V_{out}G_{m3}}{(A_3+1)G_{m1}} \tag{14}$$

$$V_y = \frac{V_{out}}{A_3+1} \tag{15}$$

Assume that the resistance of M_{res} is large enough to make the current flow through the transistor negligible. In order to keep $|V_x| = |V_y|$, the transconductance of OTA1 and OTA3 can be calculated as:

$$G_{m1} = \sqrt{(Q^2+1)}G_{m3} \tag{16}$$

As the designed OTA can achieve -50dB HD3 with 50mV input voltage, A_3 is selected to be 4. As a result, A_1 has to be 19 to make Q equal to 4. To set gain to 1, we choose $G_{m1} = G_{m2}$ and $C_2 = 3C_1 = 2.4C_3$. The center frequency can be simplified as

$$\omega_c = \frac{G_{m1}}{20C_1} \tag{17}$$

IV. 16-Channel Filter Bank Design

The bandpass filter bank covers the frequency band from 150Hz to 10kHz with 16 channels of second order gm-C bandpass filter. From 150Hz to 1kHz, the center frequencies of 8 channels are set in linear space. From 1kHz to 10kHz, the center frequencies of 8 channels are set in log space. According to (17), both OTA transconductor and filtering capacitor can be tuned to realize the 37dB frequency range.

The total output noise of bandpass filter can be calaculated as:

$$V_n^2 \approx 4nkT[\frac{1+(A_3+1)/Q}{\beta C_1} + \frac{(A_3+1)}{C_1}] \tag{18}$$

$$\beta = \frac{(A_3+1)C_2+A_3C_3}{(A_1+1)C_1} \tag{19}$$

Equation (18) shows that the output noise of the filter only decreases with the increasing value of filtering capacitor and is independent of transconductance. Therefore, the capacitors are kept the same among all channels to guarantee each channel has the identical signal to noise ratio. Considering the chip area and noise suppression at the same time, C_1 is chosen to be 1.3pF. As a result, the transconductances of OTAs alone have to cover the 37dB change. Moreover, according to (16), G_{m3} has to be about one-fourth of G_{m1}. Consequently, the total range of all G_m in the filter bank becomes 49dB. G_m of OTA in Figure 1 can be adjusted by the value of $g_{ds_{MR}}$ and M according to (3). $g_{ds_{MR}}$ is decided by the size of the M_R as well as its overdrive voltage. According to (4), the minimum value of V_{SG} has to be constrained to satisfy the harmonic distortion requirement. Therefore, the adjustable range of V_{SG} is reduced, with the ratio of maximum to minimum G_m for a fixed size of transistor M_R being 4.5 times. To implement the whole 49dB range, four OTAs with different W/L ratios of M_R and different current division ratio M are used in the 16-channel filter bank.

To eliminate the large time constant fluctuations of continuous time bandpass filter due to process variations, tuning circuitry is added to each filter. In Figure 1, the transconductance of OTA is decided by the bias current of M_2 and M_4 according to (3). The current mode tuning circuit controls the bias current of both transistors by comparing the OTA transconductance with a fixed resistor of desired value.

V. Simulation Results

The proposed filter bank was implemented on a single $1.5mm\times1.5mm$ chip in 0.5μm 3M2P CMOS technology. The source degeneration OTA is simulated in Cadence Virtuoso. Because of the fully differential structure, the second order harmonic distortion is negligible. The overdrive voltage of M_R is set to be 350mV which is the worst case of all the OTAs in the filter bank. In Figure 3, the third order harmonic distortion (HD_3) of OTA is simulated as a function of input amplitude. It can be observed that when the input peak to peak amplitude is 100mV, HD_3 of OTA is -55dB, less than 0.2%.

A block diagram of the capacitive attenuation bandpass filter is created in Matlab based on the model of designed OTA with

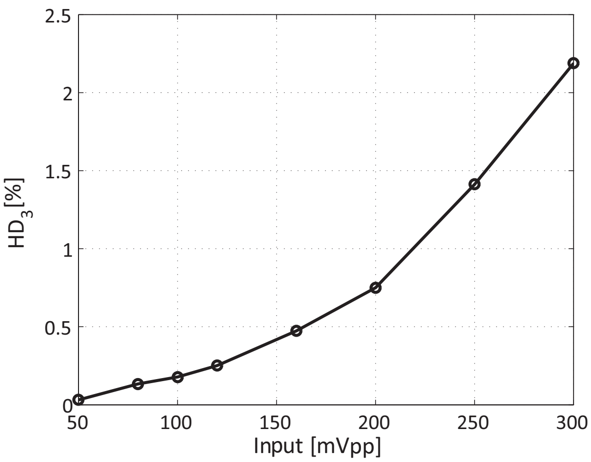

Fig. 3. Simulated HD_3 of the designed OTA as a function of the amplitude of the input signal.

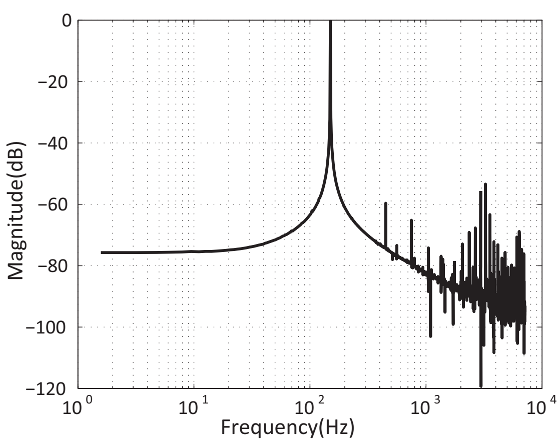

Fig. 4. Simulated output power spectrum of single channel bandpass filter with the central frequency of 150Hz.

the parameters of OTA obtained from the Cadence simulation. The simulated input referred noise is added to the OTA. A 150 Hz sinusoidal wave with 1.92 V peak to peak amplitude is used as the input signal. The HD_3 of the bandpass filter is -61.3 dB with the dynamic range of 60.2 dB.

A fully-differential single-channel bandpass filter was simulated in Cadence Virtuoso. The central frequency of the channel was 150 Hz and the peak to peak amplitude of the input signal is 1.92 V. The output power spectrum is shown in Figure 4. From the Figure, we can observe that HD_3 is -59.6 dB. Due to the smallest overdrive voltage used in 150 Hz channel, the linearity of other channels is higher.

The output noise of the bandpass filter is simulated and shown in Figure 5. The integrated output noise is 688μV, while the dynamic range is measured at 59.9 dB. The dynamic range of other channels is similar, as the same capacitor values are used in all the channels.

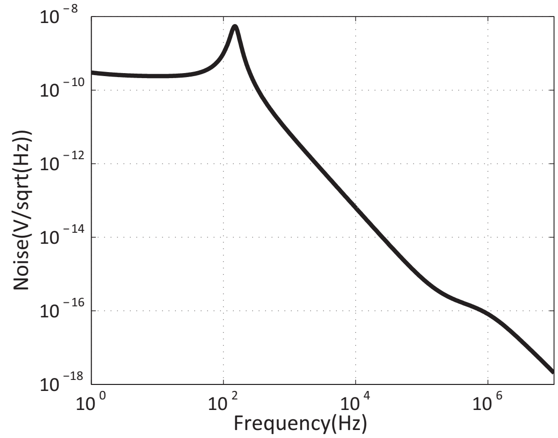

Fig. 5. Simulated output noise of BPF.

VI. Conclusion

We presented an architecture for a 16-channel filter bank that achieves high linearity and high dynamic range at low power consumption. The proposed architecture is amenable to integration in the low-power, real-time auditory microsystems for acoustic source separation for applications in smart hearing aids and acoustic tracking and surveillance systems.

VII. Acknowledgment

This work was supported by NSF CAREER Award 0846265.

References

[1] B. Edwards, "The future of hearing aid technology", *Trends Amplification*, vol. 11, no. 1, pp. 3145, Mar. 2007.

[2] C.D. Salthouse and R. Sarpeshkar. "A practical micropower programmable bandpass filter for use in bionic ears", *IEEE J. Solid-State Circuits*, vol. 38, no. 1, pp. 6370, 2003.

[3] J. Georgiou and C. Toumazou, "A 126-μW cochlear chip for a totally implantable system", *IEEE J. Solid-State Circuits*, vol. 40, no. 2, pp. 430443, Feb. 2005.

[4] S.-C. Liu, A. van Schaik, B. Minch, and T. Delbrck, "Event-based 64-channel binaural silicon cochlea with Q enhancement mechanisms", *Proc. IEEE Int. Symp. Circuits Syst.*, May 2010, pp. 20272030.

[5] S. Li and M. Stanaćević, "Subband Gradient Flow Acoustic Source Separation for Moderate Reverberation Environment," *Conf. Rec. of the 46th Asilomar Conference on Signals, Systems and Computers*, Pacific Grove CA, Nov 2012.

[6] S. Li, Y. Lin and M. Stanaćević, "Mixed-signal VLSI Microsystem for Acoustic Source Separation," *Proc. 56th. IEEE Midwest Symp. on Circuits and Systems (MWSCAS'2013)*, Columbus OH, 2013.

[7] A. J. Casson, E. R. Villegas, "A 60 pW g_mC Countinuous Wavelet Transform Circuit for Portable EEG Systems", *IEEE Journal of Solid State Circuits*, vol. 46, no. 6, pp. 1406-1415, June 2011.

[8] R. Sarpeshkar, R. F. Lyon, and C. A. Mead, "A Low-Power Wide-Dynamic-Range Analog VLSI Cochlea", *IEEE Analog Integrated Circuits Signal Process.*, vol. 16, pp. 245274, 1998.

[9] S. S. Bustos, J. S. Martinez, and F. Maloberti, "A 60-dB Dynamic-Range CMOS Sixth-Order 2.4-Hz Low-Pass Filter for Medical Applications", *IEEE Analog Integrated Circuits Signal Process.*, vol. 47, no. 12, pp. 13911398, DEC. 2000.

[10] S.-Y. Lee and C.-J. Cheng, "Systematic Design and MOdeling of a OTA-C Filter for Portable ECG Detection", *IEEE Trans. Biomedical Circuits and Systems*, vol. 3, no. 1, pp. 53-64, Feb. 2009.

[11] S. K. Arfin, "Low Power Circuits and Systems for Wireless Neural Stimulation", Ph.D thesis