Low-noise Readout IC with Integrated Analog-to-Digital Conversion for Radiation Detection System

Yingkan Lin and Milutin Stanaćević
Department of Electrical and Computer Engineering
Stony Brook University
Stony Brook, NY 11794–2350
Email: yingkan,milutin@ece.sunysb.edu

***Abstract*— A low-noise readout integrated circuit, comprising a charge sensitive amplifier, a pulse shaper with baseline holder, a peak detector and an A/D converter, is presented. The designed IC quantifies optical response of a large-area epitaxial photodiode integrated on a body of a semiconductor scintillator.The input transistor size and the time constant of the shaper are optimized to obtain a minimum equivalent noise charge(ENC) with the large input load capacitance. A time-based clockless A/D converter is implemented to minimize the interference of the digital part of the readout system on the low-noise charge-sensitive amplifier. The simulated ENC of the readout system interfacing a 50 pF capacitance and a dark current of 10 pA that model the epitaxial photodiode is 172 electrons at 12 μs time constant of the pulse shaper with power consumption of CSA and shaper of 2.2 mW.**

I. Introduction

As the threat of the illicit use of the nuclear devices or materials grows, the need for the development of more accurate radiological detection devices with localization capability becomes more critical. Semiconductor scintillating solid-state radiation detector with integrated epitaxial photodiodes on the body of scintillator, illustrated in Figure 1, guarantees nearly perfect registration of the energy of the incident radiation event [1]. Based on the Compton telescope technique, a three-dimensional array of semiconductor scintillator provides an accurate spectroscopic resolution for isotope discrimination and simultaneously an accurate determination of the direction to the source [2]. Therefore, to quantize the optical response of the epitaxial photodiode precisely, a readout ASIC integrated with the detector is necessary.

Numerous readout ASICs for radiation detection based on different sensors and applications have been studied and reported in the literature. However, most of the reported systems are designed for relatively small sensor capacitance [3], [4], with a few designed readout systems interfacing sensors with the large parasitic capacitance. A front-end ASIC for a silicon Compton telescope with 30 pF input capacitance is implemented and achieves equivalent noise charge (ENC) of 200 electrons [5]. Another readout integrated circuit interfacing avalanche photodiodes obtains an ENC as 275 electrons plus 10 electrons for every additional pico-farad of the input capacitance [6].

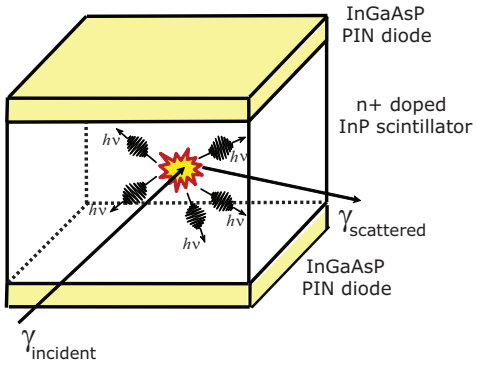

Fig. 1. Semiconductor scintillator comprising a scintillator body and an integrated photodiodes on top and bottom plates of its surface.

In the proposed semiconductor scintillator array [1], the large area of the pixel epitaxial photodiodes leads to an even larger capacitance, measured at 50 pF. Despite the large diode area, the reverse-bias leakage current is rather low, on the order of 10 pA. Accordingly, careful design of the readout system including the charge sensitive amplifier(CSA) and the pulse shaper for the proposed detector array is required to optimize the noise under power and area constraint. We have previously reported the readout IC system [7] interfacing the proposed epitaxial photodiode with the measured ENC of 950 electrons. The proposed readout system is designed with a goal of achieving a lower ENC by modifying the high-gain amplifier of the CSA and the pulse shaper. Moreover, to obtain the digital value of the output signal, an A/D converter is implemented. We propose implementation of the clockless ADC to reduce the potential effect of the switching noise on the low-noise CSA.

II. Circuit Implementation

The readout system comprises the CSA, the pulse shaper, the peak detector and the clockless ADC. The total noise of the readout system is dominated by the noise contribution of the input transistor and the sizing of this transistor is obtained through the optimization procedure [7], [8]. Due to the power constraint on the readout circuit in the proposed

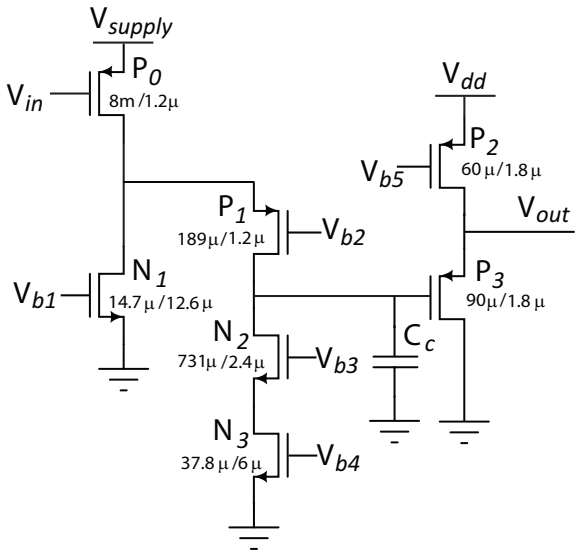

Fig. 2. Cascode amplifier with cascaded source follower as a high gain voltage amplifier in the CSA.

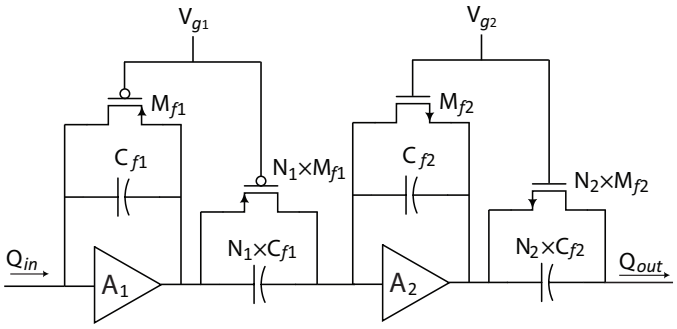

Fig. 3. Two-stage cascaded charge sensitive amplifier implementation.

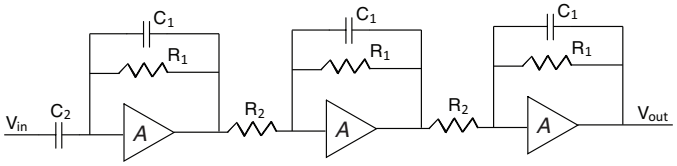

Fig. 4. Implementation of the second-order pulse shaper.

system the power of the CSA is limited to 1 mW and before the optimization of ENC, the current of the input transistor is set to 300 μA. The input transistor operates in the moderate inversion, with the channel length of 1.2 μm. The minimum ENC is obtained when the channel width is equal to 8 mm. The shaper is designed as the second order filter with the peaking time equal to the time constant. The optimal value for the peaking time is 30 μs. However, the limited chip area prohibits the implementation of a second order RC filter with that long time constant. Therefore, the actual time constant of the shaper is set to 12 μs at the cost of 20 e^- ENC increase.

A. Charge Sensitive Amplifier

A charge sensitive amplifier is composed of a voltage amplifier, a feedback capacitor and a low frequency reset network. The high gain voltage amplifier is implemented as a two stage amplifier, with the cascode amplifier followed by the source follower, as shown in Figure 2. PMOS transistor is chosen as the input transistor due to the lower flicker noise than NMOS. The input transistor P_0 has 8 mm channel width and 1.2 μm length and operates in moderate inversion. The sizing of other transistors in the amplifier is shown in Figure 2. The simulated DC gain of the amplifier is 83 dB.

A long channel MOSFET operating in the strong inversion with the value of on-resistance on the order of GΩ is used as a continuous reset network. The purpose of this reset network is to provide a DC current path and to discharge the feedback capacitor. To ensure high linearity of the CSA, a pole-zero compensation network is formed by a parallel connection of N_1 replicas of the feedback network formed by capacitor C_{f1} and transistor M_{f1}. Moreover, the compensation network converts the signal from voltage to current again, and the replica ratio N_1 determines the charge gain of this stage.

In order to achieve a high charge gain, a two-stage cascaded charge sensitive amplifier is implemented, as shown in Figure 3. The second stage has the same structure as the first stage, with the charge gain of N_2. N_1 is designed to be 20 and N_2 is 5, with the total charge gain of the CSA equal to 100.

B. Pulse Shaper with Baseline Holder

The pulse shaper is implemented as the bandpass filter with the peak value of the output voltage pulse proportional to the input charge of the CSA. The optimized time constant of the shaper is chosen to equalize the contribution of the white series noise and the white parallel noise in the output noise for the proposed CSA. In the actual implementation, a 2^{nd} order RC real pole semigaussian filter with the 12 μs time constant is designed as the trade off between required chip area and ENC. The implementation of the shaper, shown in Figure 4, is a cascade of the first-order high-pass and two first-order low-pass stages.

As the CSA and the pulse shaper are based on dc-coupling and unipolar shaping, the baseline of the output voltage signal strongly depends on the sensor leakage current. The fluctuation of the baseline of the output voltage introduces an error in the measurement of the peak amplitude. In order to maintain a stable output baseline, the baseline holder(BLH) is designed. The BLH functions as a low-frequency feedback loop around the shaper and comprises a differential amplifier, a nonlinear dynamic buffer and a low-pass filter. The low-pass filter provides the dominant pole necessary for the stability of the loop. The nonlinear buffer dynamically reduces the gain of the feedback loop only in presence of the large and fast signals. For the different sensor leakage currents, the BLH fixes the baseline voltage by adjusting the dc current according to the difference between the present baseline voltage and a reference voltage. The BLH also helps to discharge the large and fast signals to adapt the system to the high event rate.

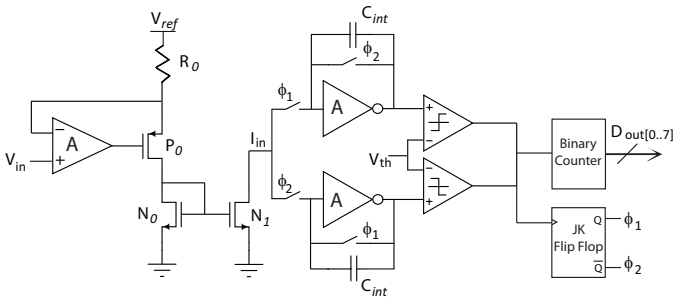

Fig. 5. Simplified schematic of the implemented clock-less A/D converter.

C. Clock-less time-based A/D Converter

In order to digitize the voltage output of the peak detector, an A/D converter is required in the readout system. A clock-less time-based A/D converter based on Wilkinson type ADC [9], [10] is implemented, as the presence of the clock in the system would interfere with the low-noise CSA. The structure of the proposed ADC that counts the number of pulses in a fixed period of time is shown in Figure 5.

The output voltage signal of the peak detector is first converted to the current, with the resistor R_0 as the linear factor in the conversion. The current is mirrored and integrated on the feedback capacitor. When the output voltage of the integrator reaches the threshold, the comparator generates a pulse to stop the counter and reset the integrator at the same time. The comparator is an open loop amplifier, with a regenerative loop introduced to speed up the response of the comparator. The digital output is equal to $[T/t_i]$, where T is a fixed time period that defines the conversion time and t_i is the time of a single cycle in which the output voltage of the integrator reaches the threshold value.

The major sources of error in the proposed structure are the reset time of the integrator t_r and the delay of the comparator t_d. Both times are unrelated to the input current. The addition of these constant times to the required integration time in each integration cycle introduces a nonlinearity in the total number of generated ramps in response to the input current. The comparator delay time is almost an order of magnitude smaller than the reset time. To significantly reduce the effect of the reset time, the non-overlapping dual integrators are implemented, as shown in Figure 5. When the first integrator reaches the threshold, the associated comparator makes the JK flip-flop toggle to activate the second integrator. Meanwhile, the capacitor of the first integrator starts discharging in preparation for the next integration cycle. The binary counter provides the sum of the number of ramps from both of the integrators. To alleviate the influence of the comparator delay, digital compensation is applied after the output N is acquired. The offset voltage of the comparator can be translated into a time delay that is related to the input current and this presents an error that is not compensated for.

The input voltage of ADC is the output voltage of the peak detector with the voltage range from 1.5 V to 3 V. The corresponding input current of the integrator after voltage to current conversion ranges from 150 nA to 5 μA. The integration capacitor is chosen to be 1 pF and the integration voltage range is 2 V. A capacitor charged by a constant current is used as the timer to generate integration time period T = 200 μs.

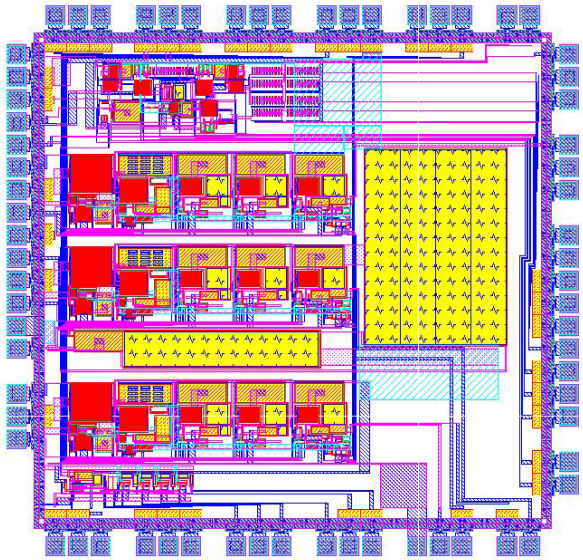

Fig. 6. Layout of the designed ASIC in 0.5 μm CMOS technology.

III. Simulation Results

The readout circuit that directly interfaces semiconductor scintillator includes the two stage CSA, the pulse shaper with baseline holder, the peak detector and the A/D converter and was simulated using Cadence SpectreS simulator. The epitaxial photodiode is modeled with a 50 pF load capacitor, a 10 pA sensor leakage current source and a current pulse generator. The power supply voltage is 3.3 V. The CSA is designed for the range of the input charge from 3,000 electrons to 100,000 electrons. This range corresponds to the predicted input charge in the proposed radiation detection application. The layout of the chip designed in 0.5μm CMOS technology with three channels of the proposed readout system is shown in Figure 6. The area that the single CSA and pulse shaper occupy is 0.42 mm^2, while the area of ADC is 0.25 mm^2. The chip is submitted for fabrication.

The output signal of the pulse shaper for different values of the input charge is shown in Figure 7. By extracting the peak value of each pulse, the linearity of the output signal as a function of the input charge is shown in Figure 8. The charge gain of the readout system is 86.5 mV/fC. Figure 9 shows the simulated ENC for different values of the input capacitance. When the input capacitance is 50 pF, the simulated ENC is 172 electrons, as predicted by the optimization procedure.

An 8-bit ADC with input range from 1.5 V to 3 V is simulated, and the integral nonlinearity(INL) of the ADC after the digital compensation for the comparator delay is shown in Figure 10.

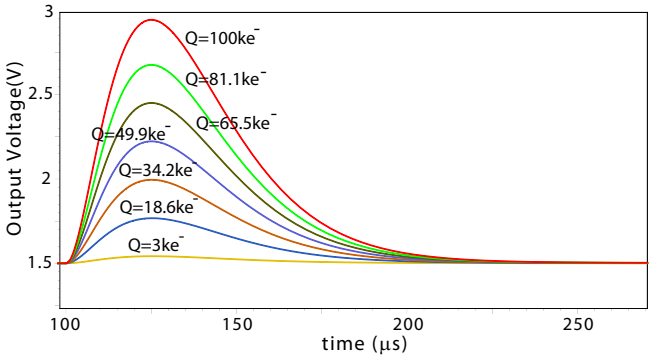

Fig. 7. Output transient response of the pulse shaper with different input charge.

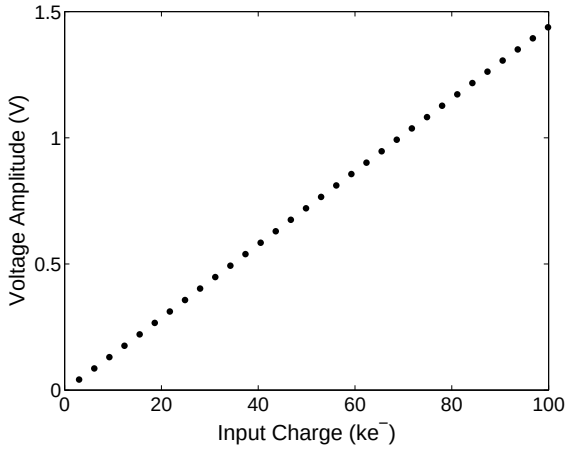

Fig. 8. Linearity of the output signal of the pulse shaper for different input charge.

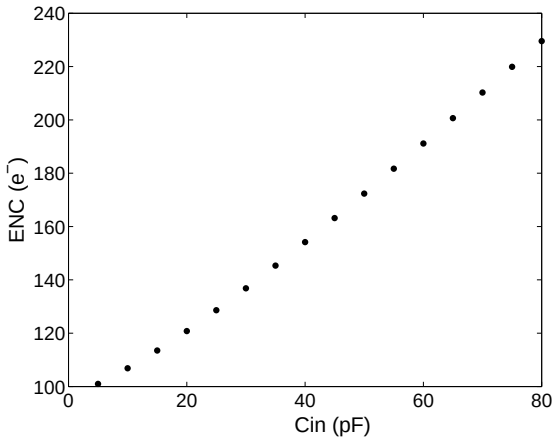

Fig. 9. ENC as a function of the input capacitance.

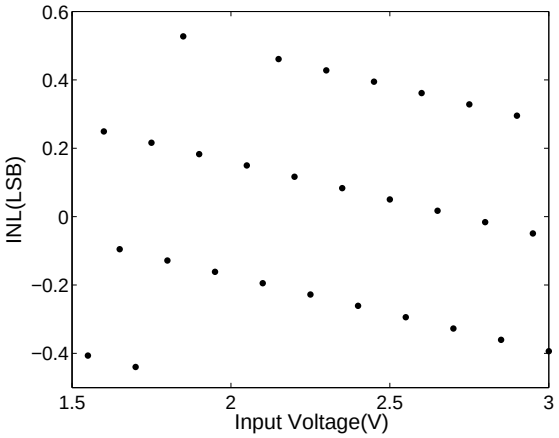

Fig. 10. INL of the clockless A/D converter.

IV. Conclusion

A charge amplification interface circuit followed by a clockless A/D converter is proposed as a readout system for a large-area epitaxial photodiode. By optimizing the size of the charge amplifier input transistor as well as the time constant of the pulse shaper, the simulated ENC of the readout IC is reduced to 172 electrons with a 50 pF input load capacitance. The 8-bit time-based ADC converts the output of the peak detector proportional to the input charge to digital value while minimizing interference on the low-noise CSA. To experimentally verify the performance of the circuit, a prototype chip has been fabricated in the 0.5μm CMOS technology.

Acknowledgment

This work was supported by the Domestic Nuclear Detection Office (DNDO), Department of Homeland Security.

References

[1] S. Luryi, A. Kastalsky, M. Gouzman, N. Lifshitz, O. Semyonov, M. Stanacevic, A. Subashiev, V. Kuzminsky, W. Cheng, V. Smagin, Z. Chen, J.H. Abeles and W.K. Chan, "Epitaxial InGaAsP/InP photodiode for registraion of InP Scintillation", *Nucl. Instrum. Methods Phys. Res. A*, vol. 622, pp. 113-119, 2010.

[2] S. Luryi and A. Subashiev, "Semiconductor scintillator for 3-dimensional array of radiation detectors", *Future Trends in Microelectronics : Unmapped Roads*, Wiley Interscience, pp. 331-346, 2010.

[3] G. De Geronimo, P. O'Connor and J. Grosholz, "A Generation of CMOS Readout ASICs for CZT Detectors", *IEEE Tran. Nucl. Sci.*, vol. 47, no. 6, pp. 1857-1867, 2000.

[4] C. Fiorini and M. Porro, "DRAGO Chip: A Low-Noise CMOS Preamplifier Shaper for Silicon Detectors With Integrated Front-End JFET", *IEEE Trans. Nucl. Sci.*, vol. 52, no. 5, pp. 1647-1653, 2005.

[5] G. De Geronimo, J. Fried and E. Frost, "Front-end ASIC for a silicon compton telescope", *IEEE Trans. Nucl. Sci.*, vol. 55, no. 4, pp. 2323-2328, 2008.

[6] X. C. Fang, Ch. Hu-Guo and N. Ollivier-Henry, "Design of a Multi-Channel Front-End Readout ASIC with Low Noise and Large Dynamic Input Range for APD-Based PET Imaging", *IEEE Tran. Nucl. Sci.*, vol. 57, no. 3, pp. 1015-1022, 2010.

[7] X. Yun, M. Stanacevic and S. Luryi, "Low-Power Amplifier for Readout Interface of Semiconductor Scintillator", *IEEE Trans. Nucl. Sc.*, vol. 58, no. 4, pp. 2129-2136, 2011.

[8] G. De Geronimo and P. O'Connor, "MOSFET optimization in deep submicron technology for charge amplifiers", *IEEE Trans. Nucl. Sci.*, vol. 52, no. 6, pp. 3223-3232, 2005.

[9] M. S. Emery, S. S. Frank, J. Britton and A. L.Wintenberg, "A multichannel ADC for use in the PHENIX detector", *IEEE Trans. Nucl. Sci.*, vol. 44, no. 3, pp. 374-378, Jun. 1997.

[10] A. Rossini, S. Caccia and G. Bertuccio, "A complete read-out channel with embedded Wilkinson A/D converter for X-ray spectrometry", *IEEE Trans. Nucl. Sci.*, vol. 54, no. 3, pp. 1216-1221, Aug. 2007.