A Low-Power Wide-Dynamic-Range Readout IC for Breath Analyzer System

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***Abstract*— We present a low-power wide-dynamic-range readout circuit that directly interfaces a selective metal-oxide gas sensor. The proposed novel readout architecture implements an adaptive baseline compensation and limits the sensor current. The readout IC can interface the sensors with the baseline resistance from 1 kΩ to 100 MΩ and measures the gas induced resistance change in the range from 0.05% to 10% of the baseline resistance. The simulations demonstrate the 166 dB dynamic range of the readout circuit and 113 μW power consumption amenable to the sensors that can operate at room temperature for the application of the proposed system in portable breath analyzers.**

I. Introduction

Detection and discrimination of the signaling metabolites in the exhaled breath and their measurement in the trace concentrations would lead to a personal breath analyzer, a fast, non-invasive and early diagnostic medical tool [1], [2]. The sensitivity required for quantification of the parts-per-billion level concentration of these signaling metabolites calls for novel circuit and system techniques in the design of the readout IC system. To achieve the high sensitivity, readout techniques have to address inherent properties of the sensor, particularly their large baseline resistance that can be few orders of magnitude higher than the actual sensor response, large variability of base resistance across sensors, and the drift in base resistance over time at a different rate across sensors.

There is a wide range of proposed instrumentation techniques developed for resistance measurement in the literature [3], [4], with the readout IC that achieve the accuracy down to 0.1% by tracking baseline resistance [5], [6]. Apart from satisfying the sensitivity and dynamic range requirements in the presence of the large variable baseline resistance for the readout system, power consumption is important design constraint for the systems containing sensors that can operate at the room temperature.

We propose a low-complexity low-power architecture for the measurement of gas concentrations that tracks the baseline resistance. The readout circuit matches the sensor baseline resistance from 1 kΩ to 100 MΩ. The detectable resistance change ratio ranges from 0.05% to 10% of the base resistance, which leads to the dynamic range of the system of 166 dB. In addition, the power consumption of the systems is significantly reduced compared to the solutions proposed in the literature. The proposed topology is also amenable to implementation of the signal processing algorithms based on the independent component analysis [7] that can compensate for the variation of the baseline resistance of the sensor due to degradation and aging.

II. Readout Circuit Architecture

The proposed gas-sensing system consists of three main parts: an array of gas sensors, an electronic readout circuit and a data processor. Each gas sensor behaves electrically as a resistor. The electrical resistance of each of the sensors in the array is composed of two series resistances. The first series resistance is a baseline resistance, R_b. The baseline resistance varies across sensor design and even across sensors with the same design. The value of this resistance can be in a wide range that spans over several decades. Due to ageing of the device and temperature gradient, this baseline resistance also demonstrates change over time. The second component of the sensor resistance is the resistance related to the presence of the specific gas in the environment, ΔR_{gas}. Thus, the total resistance of a gas sensor in the array is given by:

$$R_{sense} = R_b + \Delta R_{gas}, \tag{1}$$

where only ΔR_{gas} represents the useful signal, as the ratio of ΔR_{gas} and R_{sense} quantifies the existence and density of the target gas.

Gas sensors that are sensitive to only a specific class of gaseous analytes or even specific to a single gas are produced through control of the microstructure or temperature of semi-conducting metal oxide thin films [1]. The baseline resistance of these sensors spans over 5 decades, from 1 kΩ to 100 MΩ. In the presence of gas analytes, the estimated range of the resistance ΔR_{gas} varies from 0.05% to 10% of the baseline resistance R_b, leading to the total dynamic range of resistance R_{sense} of 166 dB.

We propose implementation of a readout system that is insensitive to the baseline resistance and measures only the gas induced resistance change in a specific range around the baseline resistance. The system block diagram is shown in Figure 1. A voltage D/A converter and a current D/A converter are introduced to compensate for the baseline resistance and to limit the power consumption. The current D/A converter (IDAC) is used for cancelation of the baseline resistance of sensor through calibration. The voltage D/A converter (VDAC) provides for a different voltage drop across the sensor and effectively limits the current that flows through the sensor, that is the power consumption of the readout system. The

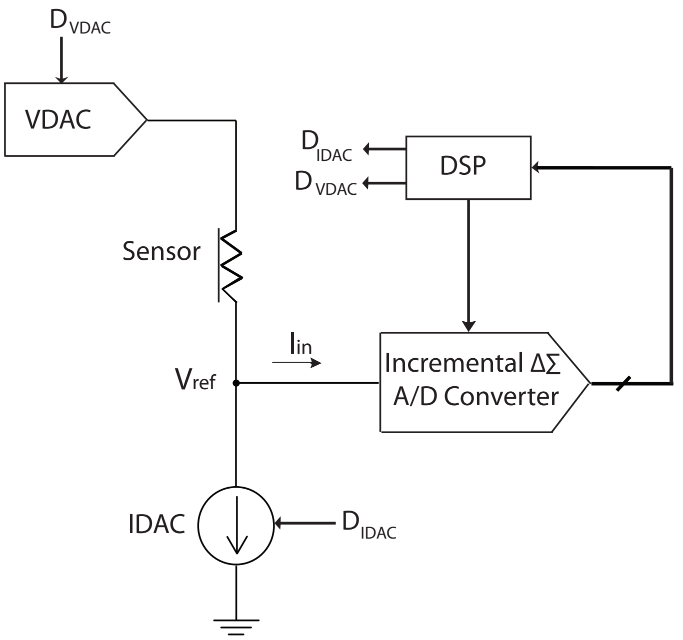

Fig. 1. Block diagram of the proposed readout system.

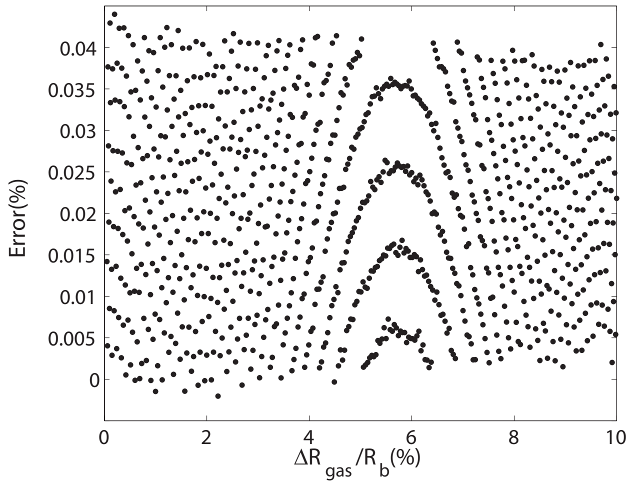

Fig. 2. The relative measurement error as the function of the ratio of the gas induced change in the sensor resistance ΔR_{gas} and the baseline resistance R_b. The baseline resistance is set to the maximum value of 100 MΩ.

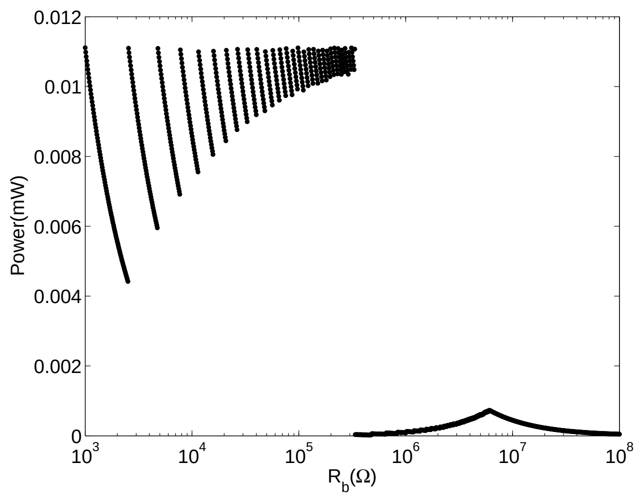

Fig. 3. Power consumption of the readout system as the function of the baseline resistance when the ratio of the gas induced change in the sensor resistance ΔR_{gas} and the baseline resistance R_b is 10%.

difference between the current that flows through the gas sensor and current of D/A converter (IDAC) is measured by the A/D converter, implemented as the current mode incremental $\Delta\Sigma$ converter. The measured current corresponds to the component of the sensor resistance sensitive to the change in the gas concentration. As the large portion of the sensor current that originates from the baseline resistance is compensated by IDAC, the required resolution of the current ADC is significantly reduced and only moderate resolution is required. In this way, by adjusting the digital input value of the two D/A converters, the interface circuit can be both energy efficient and highly accurate.

In the proposed system implementation, D/A converters are designed as 5-bit voltage DAC and 8-bit current DAC with two scales that correspond to the baseline resistance ranges from 1 kΩ to 320 kΩ and from 320 kΩ to 100 MΩ. The V_{ref} is set to 0.9 V, while the voltage range of the voltage DAC is from 1 V to 2.9 V. The voltage range of the DAC limits the maximum current through the sensor to 110 μA. The designed resolution of the current ADC is 13 bits with two measurement ranges. The least significant bit of two current ranges are 9 pA and 2.85 nA. To demonstrate the accuracy and power consumption of the proposed system architecture, the system is simulated in MATLAB. The simulation is run from the calibration phase to the sensor resistance measurement. In Figure 2, the baseline resistance is chosen to be 100 MΩ, which is the worst case scenario for the sensitivity of the system due to the smallest sensor current. The change in the sensor resistance is from 0.05% to 10% of the baseline resistance. From the Figure 2, we can observe that the maximum error is on the order of 0.045% of the baseline resistance. To quantify the power consumption of the system, sensor resistance change ratio is fixed at 10% which incurs the largest current variation. Figure 3 shows the power consumption as a function of the baseline resistance at this sensor resistance change ratio.

A. Calibration Process

The proposed readout circuit topology has two modes of operation, namely calibration and conversion. Calibration is used to set the voltage across the sensor to a constant reference voltage in the absence of the gas, as the baseline resistance varies across the sensors. Thus calibration sets the biasing current of current DAC to a constant value before data conversion. The calibration not only guarantees high accuracy with a moderate resolution of ADC, but also limits the power consumption of the readout system.

Since the expected value of the baseline resistor (R_b) is known before the calibration begins, the scale of ADC and

IDAC can be determined by comparing the expected R_b with the boundary resistance between two scales, 320 kΩ. At the same time, the input value of the VDAC can also be set according to R_b. Therefore, during the calibration phase, only the input of the IDAC has to be determined. In this process, the ADC works as a comparator in a 1 bit mode and the output bit represents the direction of the input current. According to Figure 1, by increasing the output current of the IDAC, the current flowing into the ADC is decreasing until the current direction changes. At that moment, the input current of the ADC is less than 1 LSB of IDAC, and the calibration is completed.

III. Circuit Implementation

The readout system shown in Figure 1 consists of a 8-bit current D/A converter, a 5-bit voltage D/A converter and a 13-bit current A/D converter. In the following section, we present the circuit implementation of the current D/A and current A/D converter.

A. Incremental $\Delta\Sigma$ ADC

The choice of the current-measuring first-order single bit delta-sigma modulator matches the low-frequency content of the signal of interest, which allows high oversampling ratios and trade-off between bandwidth and resolution, and offers additional noise reduction [8]. The incremental delta-sigma ADC used in the system comprises the current integrator, the comparator and the switched-current single-bit D/A converter. The implementation of the integrator and the switched-current DAC is shown in Figure 4.

The input current is integrated onto a capacitor in the feedback loop of a single-ended, high-gain amplifier. The high-gain amplifier is implemented as a telescopic cascode amplifier with the input transistor operating in a subthreshold regime. A pair of integrating capacitors C_1' and C_1'' are selected according to the current scale of the ADC and their values are 100 fF and 1.9 pF, respectively. Their values are decided by the LSB current, sampling and system clock frequency. The sampling frequency of the ADC is set to 100 Hz, which corresponds to the slow-changing gas detection environment. The integrator clock $intClk_1$ and $intClk_2$ are non-overlapping inverting clocks with sampling frequency. The clock $intClk_{1e}$ is the replica of $intClk_1$ with late rising edge and early falling edge to alleviate the charge injection. Correlated double sampling (CDS) establishes the voltage at the virtual ground input to the integrator through a coupling capacitor C_2 inserted between the integrator input and the amplifier. C_2 is chosen to be 1 pF to minimize the effect of the charge leakage over the duration of the conversion cycle. After integration, the output voltage of the integrator is compared with the mid-level voltage, and the difference between them is amplified and latched by the D flip-flop to determine the direction of the reference current in the next clock cycle.

B. Current Mode D/A Converter

The current mode D/A converter of the system is implemented using segmented current-steering structure [9]. This structure can make use of the advantages offered by both binary-weighted and thermometer-coded current DAC architecture. With thermometer-coded bits, DAC is guaranteed monotonicity, good differential nonlinearity and very low glitches. However, it suffers from complexity, large area and power consumption. The binary-weighted structure consumes the small chip area and the power but does not guarantee monotonicity and good differential nonlinearity. The segmented current-steering implementation of a 8-bit current mode D/A converter separates input data into 4 more-significant bits in thermometer-code controlling equal current sources and into 4 less-significant bits with binary-weighted current sources, as shown in Figure 5. For the sizing of the transistors in 0.5 μm CMOS technology, we used for the standard deviation of threshold voltage $\sigma(\Delta V_T)$ value of 0.43 mV and for standard deviation of the current factor $\sigma(\Delta\beta)$ value of 0.04. The optimized current source size based on these values is W/L=18μm/36μm.

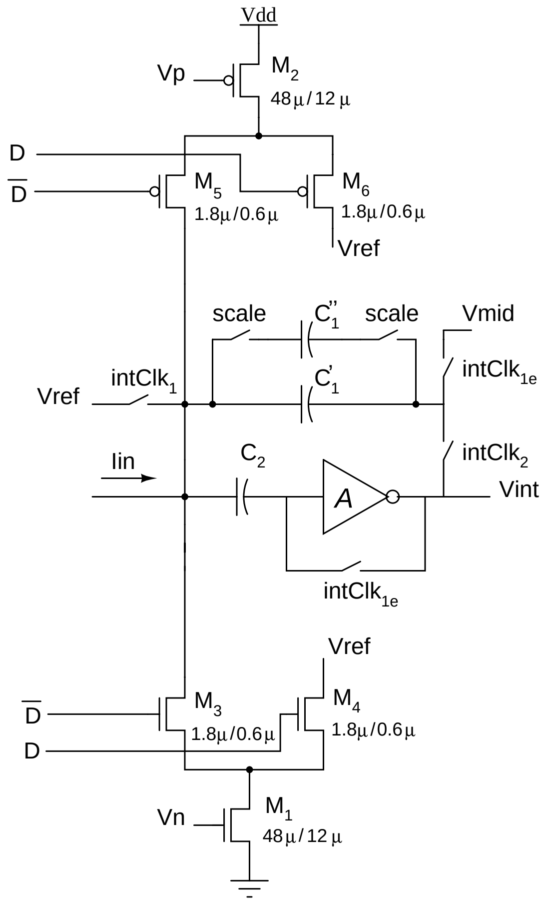

Fig. 4. Schematic of the current integrator in the implemented incremental delta-sigma modulator.

IV. Simulation Results

The current 13-bit incremental delta-sigma ADC and 8-bit current DAC were simulated using Cadence SpectreS simulator. For the simulation of ADC, 17 points are selected from the input current range from -18 nA to 18 nA. The

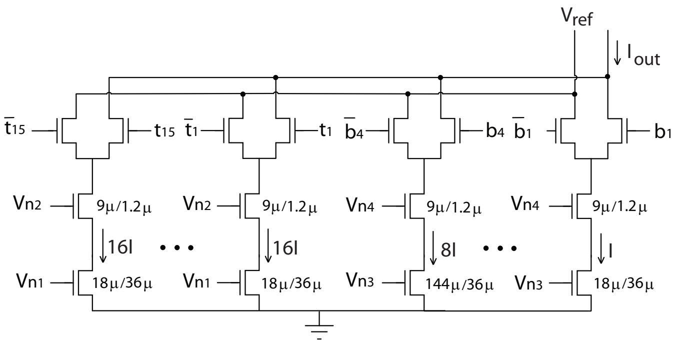

Fig. 5. Schematic of the segment current mode D/A converter.

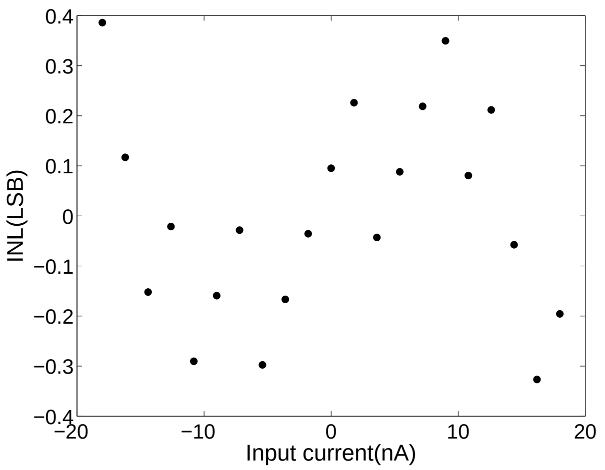

Fig. 6. The integral nonlinearity (INL) of the current-mode incremental $\Delta\Sigma$ ADC.

system clock is set at 1 MHz and the feedback capacitance is 100 fF. I_{lsb} for this current range is equal to 9 pA. The integral nonlinearity (INL) error is shown in the Figure 6. For the simulation of current D/A converter, 30 points are selected in the current range from 0 to 100μA. I_{lsb} for this current range is equal to 400 nA. The linearity of the IDAC is shown in the Figure 7.

As demonstrated in Figure 3, the power consumed in the sensor is limited to less than 12 μW for the lowest possible sensor resistance, while in this case the power consumption of the current DAC is equal to 91 μW. The power consumption of the voltage DAC and the incremental delta-sigma ADC are simulated at 10 μW. Therefore, the total power consumption of the system is in the worst case 113 μW, which is by two orders of magnitude lower than previous solutions proposed in the literature with the similar dynamic range.

V. Conclusion

The proposed readout IC system compensates for the variation in the baseline resistance and reduces the necessary resolution of ADC without sacrificing accuracy. The interface circuit is compatible to the sensor baseline resistance from 1 kΩ to 100 MΩ and guarantees error rate less than 0.045%. The system achieves low power consumption on the order of 100 μW. With the achieved performance, the readout system can be integrated with selective gas sensor array into a handheld breath analyzer. As coarse diagnostic tool, the envisioned breath analyzer may provide the first detection device and direct a more complex diagnostic tools. Personal breath analyzer could also be of great significance in the case of emergency diagnostic, where due to chemical or biological threat, the time of detection and priority of possible victims can be of essence in the response to such threat.

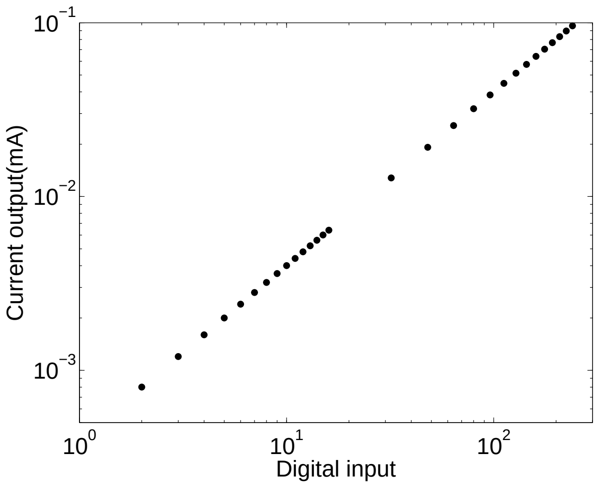

Fig. 7. The output linearity of the current mode D/A converter.

Acknowledgment

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