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3-D Integrated Implantable Device for Deep Brain Sensing and Stimulation

Form factor is a key design objective in implantable biomedical devices. A smaller form factor, therefore a tinier implant, not only mitigates issues encountered during the implantation process, but also provides a more robust and longer *in vivo* monitoring capability since the microsystem is less sensitive to body movements [1]. This issue of physical area is exacerbated for deep brain implants where the site of implantation is critical.

Invasive deep brain implants, located under the skull, monitor and record neural activities in specific locations of the brain. These data are analyzed to identify certain neural patterns, thereby providing highly valuable information to better understand the operation of brain and diagnose brain diseases. Furthermore, brain implants are also used for stimulation by transmitting electrical impulses to specific parts of the brain. Thus, deep brain stimulation is a crucial part of neural prostheses and can potentially heal disorders such as Parkinson's and Alzheimer's diseases, brain injury, and paralysis. Future brain implants therefore have an ambitious, albeit inspiring, goal of observing the brain activity, decoding the extracted neural information, and ultimately restoring the disabled function to the body. While such a goal brings significant challenges in diverse fields such as the fabrication of highly parallel nanoscale sensors/actuators and biocompatibility, this work focuses on a low form factor implantable integrated circuit (IC) design by exploiting monolithic 3-D integration technology.

While the use of IC technology has been widely utilized to realize smaller implants [2], these efforts have concentrated on traditional planar IC technologies. In the past decade, three-dimensional (3-D) integration has emerged as a promising technology to achieve higher integration density and reduce the global interconnect length [3]. Existing work in 3-D technology focuses on high performance computing applications such as processor-memory stacks. As opposed to the conventional practice, 3-D integration is exploited in this work *to reduce the form factor* in deep brain implants.

In a monolithic 3-D circuit, multiple heterogeneous planes are stacked where dense through silicon vias (TSVs) are utilized to achieve vertical communication among the planes, as shown in Fig. 1

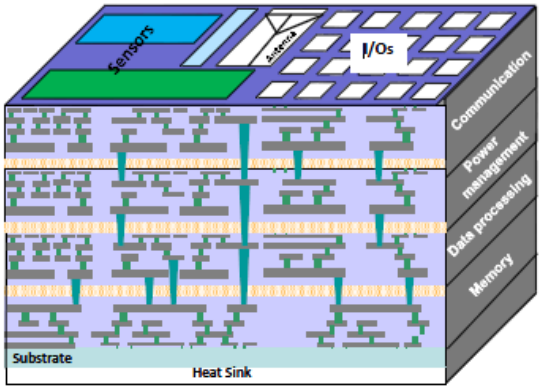

Figure 1: Monolithic 3-D integration technology where through silicon vias (TSVs) are utilized to achieve communication among the planes.

This hybrid integration capability is highly advantageous for implantable applications since each plane can be individually optimized based on the required function and design objectives. For example, the communication plane is designed with physical parameters that enhance the realization of on-chip passive devices, a primary limitation for implantable devices. Furthermore, the overall area of the system is reduced, achieving a smaller form factor. For example, in [2], the entire area of the proposed neural interface chip consisting of a rectifier, voltage regulator, clock recovery circuitry, analog-to-digital converter,

neural amplifier, spike detectors, and a wireless data transmitter occupies an area of approximately 30 mm^2. Assuming a six plane 3-D stack, the area can be reduced to approximately 12 mm^2, achieving 60% reduction.

As the first step in exploiting 3-D technology for deep brain implants, we map a previously designed and fabricated potentiostat, shown in Fig. 2, to a two plane 3-D architecture and analyze the noise coupling and signal integrity characteristics. A multichannel potentiostat, integrated with microfabricated sensor array, is used for distributed simultaneous monitoring of neurochemical activity [4]. Despite the advantage of reducing the area and achieving a smaller form factor, a 3-D integrated implantable device suffers from significant noise coupling due to dense integration and TSV characteristics, as demonstrated in this work.

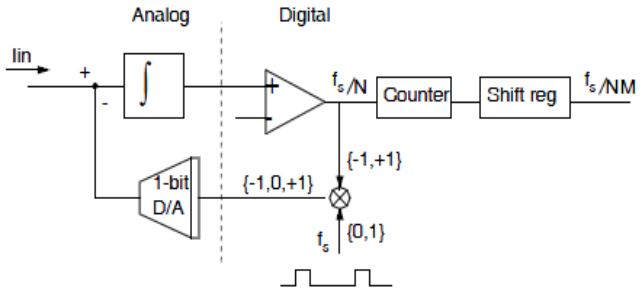

Figure 2: System level diagram of a single channel of the potentiostat.

Electrical models are first proposed to analyze noise characteristics in both 2-D and 3-D integrated potentiostat. The models include the substrate, power/ground networks, and TSVs. The proposed electrical models are combined with the circuit schematic in 0.5 µm CMOS technology. The overall netlist is simulated in Spectre using Cadence IC design tools. Some of the results are summarized in Table 1.

TABLE I
RMS VALUE OF THE NOISE AT THE BULK NODE OVER 10 μS FOR DIFFERENT CASES.

Case	RMS noise at the bulk node
2-D common power network	232 μV
2-D dedicated power network	224 μV
3-D nonideal TSV	242 μV
3-D ideal TSV	107 μV

Signal integrity analysis of a 2-D and 3-D integrated potentiostat produces important conclusions: (1) in a 3-D integrated potentiostat, clock TSVs with short rise times inject significant noise into the substrate of the analog plane since these signals need to reach the bottom plane where the digital circuit is located, (2) this coupling mechanism is due to the TSV-to-substrate capacitance of the TSVs, (3) the distance between an aggressor TSV and a victim device should be carefully considered, (4) efficient and 3-D specific noise isolation strategies should be developed, (5) contrary to the common assumption and despite having two separate substrates, 3-D systems do not necessarily exhibit superior noise performance due to TSV related noise coupling. Ignoring this noise coupling mechanism produces 3-D implantable devices with significantly poor signal integrity characteristics.

References

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