# Low-power Charge Sensitive Amplifier for Semiconductor Scintillator

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***Abstract*— A design of low-noise charge sensitive amplifier (CSA) for measurement of optical response of photo-detector registering light produced by semiconductor scintillator is presented. Detailed analysis of the CSA suitable for large parasitic detector capacitance is provided, regarding noise, power and stability. Two scenarios where input transistor is biased in strong inversion and weak inversion are compared, with included accurate $1/f$ noise modeling. The experimental prototype was implemented in 0.5$\mu$m CMOS process with a 5 V power supply.**

## I. Introduction

There is a great need for enhancement of the effective integration of nuclear and radiological detection capabilities in order to prevent illicit use of nuclear devices or materials. A proposed three-dimensional (3D) integration of scintillation-type semiconductor detector pixels provides accurate spectroscopic resolution for isotope discrimination and an accurate determination of the direction to source at the same time [1]. In novel scintillation-type semiconductor detector high energy radiation produces electron-hole pairs in a direct-gap semiconductor material that subsequently undergo interband recombination, producing infrared light to be registered by a photo-detector. To measure the optical response of pixelized detector, an application specific integrated circuit has to be designed. A significant design challenge for the ASIC is the large parasitic capacitance of the sensor, which for the pixel size of $1mm$ x $1mm$ in the proposed photodetector is measured to be 50 pF. Detailed analysis of optimization of charge sensitive amplifier(CSA) for large parasitic capacitance with constraints on power consumption and limiting area is presented.

## II. Noise optimization

The system block diagram of readout system that directly interfaces photodetector is shown in Figure 1. A CSA is the most important component of a front-end readout system and requires detail optimization procedure. Figure 2 shows the folded-cascode amplifier as the assumed structure for CSA. The detector generates a certain amount of charge $Q$ in a very short time period, normally in nS range. The generated charge is integrated onto a small feedback capacitance $C_f$, which creates a voltage step signal at the output with an amplitude equal to approximately $Q/C_f$.

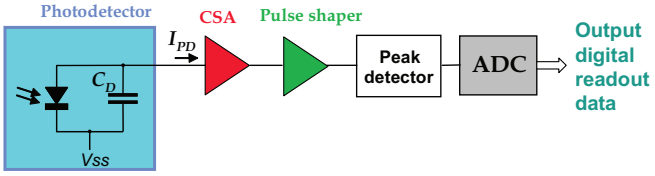


Fig. 1. Block diagram of proposed system

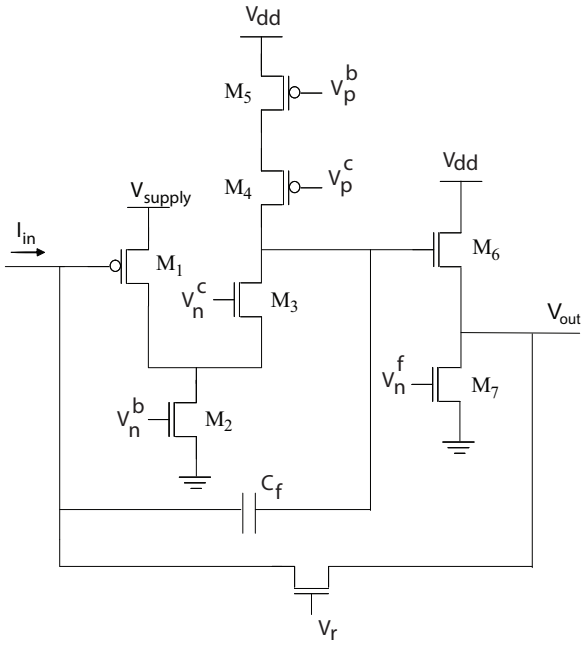


Fig. 2. Schematic of CSA

### A. Input transistor optimization

The sensitivity of readout system is expressed through equivalent noise charge (ENC) [2]. ENC comprises of three main components white series noise, originating from input MOS thermal noise, flicker noise, and white parallel noise, due to the detector leakage current and the feedback network:

$$ENC_{ws}^2 = a_{ws}\frac{\gamma}{g_m}(C_p + C_g)^2\frac{1}{\tau} \quad (1)$$

$$ENC_{wp}^2 = a_{wp}I_{det}\tau \quad (2)$$

$$ENC_{1/f}^2 = a_f K_F (C_p + C_g)^2 \quad (3)$$

where $a_{ws}$, $a_{wp}$ and $a_f$ are the constant shaping factors that depend on the order of pulse shaper; $\gamma$ is the thermal noise coefficient that depends on the operation region of transistor; $g_m$ and $C_g$ are the transconductance and gate capacitance of input MOS transistor; $C_p$ is the load capacitance at the CSA input, which includes the detector parasitic capacitance; $\tau$ is the time constant of the following shaper; $I_{det}$ is the detector leakage current and $K_F$ is integrated flicker noise contribution of input transistor.

The flicker noise of MOS transistor has two different origins [3], [4]. The $\delta N$ model assumes the drain noise current is a result of fluctuation of charge carriers. The $\delta\mu$ model assumes that the fluctuation of charge carriers mobility generates the noise. Studies have shown that p-MOSFET generally follows the $\delta N$ model when biased in weak inversion, and the $\delta\mu$ model when biased in strong inversion. Therefore, the 1/f flicker noise voltage spectral density $S_F$ can be expressed as:

$$S_{F,\delta N} = (\frac{q^2 nkTN_T}{2\beta C_{ox}^2})\frac{1}{WL}\frac{1}{f} \tag{4}$$

$$S_{F,\delta\mu} = (\frac{nq\alpha_H}{\sqrt{2\mu C_{ox}^3}})(\frac{1}{\sqrt{W^3 L}})\sqrt{I}\frac{1}{f} \tag{5}$$

where $n$ is the subthreshold slope coefficient, $\alpha_H$ is the Hooge constant, $N_T$ is the oxide/interface trap density per unit volume and energy at the quasi Fermi level, $\beta$ is the tunneling parameter of the traps, $I$ is the biasing current of input transistor. It is seen that the $\delta\mu$ model predicts the noise increases with the root square of biasing current $I$, while the $\delta N$ model predicts that the noise is independent of $I$. As of this reason, optimization is formulated under two different conditions, strong inversion and weak inversion of input transistor region of operation.

*1) Strong inversion:* By inserting value of transconductance of transistor biased in strong inversion in (1) and spectral density model of $1/f$ noise in (3), we obtain

$$ENC_{ws}^2 = (\frac{a_{ws}}{\tau}\frac{\gamma L}{q^2\sqrt{2\mu/n}})\frac{(C_p+C_g)^2}{\sqrt{C_g}}\frac{1}{\sqrt{I}} \tag{6}$$

$$ENC_{1/f}^2 = (a_f\frac{nq\alpha_H L}{\sqrt{2\mu}})\frac{(C_p+C_g)^2}{\sqrt{C_g^3}}\sqrt{I} \tag{7}$$

Thus, the total ENC is expressed in terms of three design variables: biasing current $I$, gate capacitance of input transistor $C_g$ and shaping constant $\tau$. Optimum $I$ exists as $ENC_{ws}$ decreases with $I$ while $ENC_{1/f}$ increases with $I$. Optimum $\tau$ exists as $ENC_{ws}$ and $ENC_{wp}$ share the same relation. The constraints on the optimization of ENC originate from rate of the events, that presents the upper bound on the choice of $\tau$, total power consumption of CSA, that constraints the biasing current and the chip area, that presents constraint for choice of $C_g$. For our detector with $50pF$ parasitic capacitance and $10pA$ leakage current, unconstraint optimization leads to minimum ENC of $50e^-$ at a biasing current of $21mA$, which is significantly over the power consumption limit of our system. There is also additional constraint that links choice of biasing current and gate capacitance, related to the operation region of the input transistor, and can be derived from condition of transistor operating in strong inversion

$$I > 5I_S, \tag{8}$$

with

$$I_s = 2n\mu C_{ox}U_T^2\frac{W}{L}, \tag{9}$$

where $U_T$ is the thermal voltage. This leads to upper bound on size of transistor

$$C_g < \frac{IL^2}{10n\mu U_T^2}. \tag{10}$$

For the range of applications we are interested in, the rate of events is low, and the optimal shaping constant can be lower than $1ms$. This leads to unconstraint optimization of $\tau$ and closed form for optimal value derived as

$$\tau_{op} = \sqrt{\frac{a_{ws}\gamma}{a_{wp}I_{det}}}(\frac{C_p+C_g}{\sqrt{g_m}}) \tag{11}$$

Assuming this optimum $\tau$ is feasible, the total ENC can be derived as

$$ENC_{strong}^2 = A_1 I^{-\frac{1}{4}}\frac{C_p+C_g}{Cg^{\frac{1}{4}}} + A_2\sqrt{I}\frac{(C_p+C_g)^2}{C_g^{\frac{3}{2}}} \tag{12}$$

where $A_1$ and $A_2$ are constants that can be derived from previous equations. Minimum thermal noise would be achieved for $C_g = 1/3C_p$, while the minimum flicker noise is achieved for $C_g = 3C_p$, if thermal and flicker noise would be independently optimized.

*2) Weak inversion:* Transistor biased in weak inversion has the highest $g_m/I_d$ ratio, therefore it is desired to bias the transistor in weak inversion for applications that have tight power budget. ENC for the case of input transistor operating in weak inversion can be obtained by inserting the value of transconductance in (1) and $\delta N$ model for 1/f noise in (3)

$$ENC_{ws}^2 = \frac{a_{ws}\gamma nkT}{Iq}(C_p+C_g)^2\frac{1}{\tau} \tag{13}$$

$$ENC_{1/f}^2 = a_f(\frac{q^2 nkTN_T}{2\beta C_{ox}})\frac{(C_p+C_g)^2}{C_g} \tag{14}$$

Optimum $\tau$ still exists, while optimum $I$ is chosen as the largest current that keeps the input transistor in weak inversion. The total ENC can be derived in a similar way as for strong inversion, when there is no limit on $\tau$:

$$ENC_{weak}^2 = B_1\frac{C_p+C_g}{\sqrt{I}} + B_2\frac{(C_p+C_g)^2}{C_g} \tag{15}$$

where $B_1$ and $B_2$ are still constants that can be derived from previous equations. The minimum thermal noise is achieved at lowest $C_g$ while $C_g = C_p$ is minimum for flicker noise. Now the gate capacitance has a lower bound starting from relationship

$$I < 0.1I_S, \tag{16}$$

and leading to

$$C_g > 5IL^2/n\mu U_T^2 \tag{17}$$

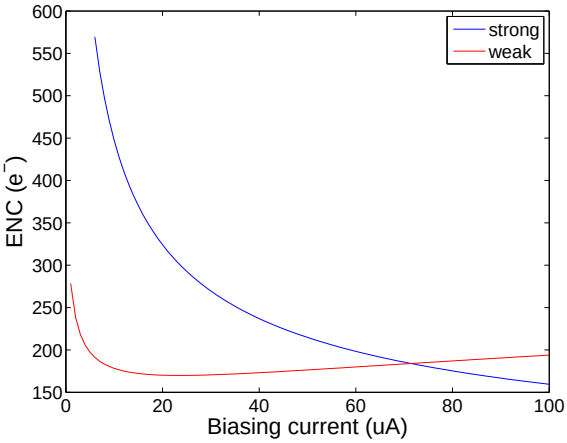


Fig. 3. Optimized ENC as a function of biasing current under strong and weak inversion.

*3) Weak inversion and strong inversion comparison for fixed current:* When absolute minimum noise is desired, the transistor would be biased in strong inversion. However, in circumstances where the biasing current of input transistor is fixed due to limited power budget, the optimization process is modified and choice of region of operation of the transistor depends on the required power consumption. Figure 3 shows the minimum achievable ENC for a fixed biasing current if the transistor operates in strong inversion or weak inversion. In strong inversion, ENC monotonically decreases as current increase.Since the input transistor cannot be large enough to fall into the range of $1/3C_p < C_g < 3C_p$, due to the relative small biasing current, the minimum ENC is always achieved when $C_g$ is the largest value that keeps the input transistor in strong inversion. In weak inversion, a minimum ENC exists when $0 < C_g < C_p$. The minimum point corresponds to the previous results. As can be seen from the figure, when biasing current is limited to about tens of $\mu A$, weak inversion is advantageous over strong inversion; when biasing current moves to above $100\mu A$, strong inversion becomes more preferred.

### B. CSA optimization

The additional noise contributions from $M_2$, $M_3$ and $M_5$ can be approximated as:

$$V_{n,add}^2 = (V_{n2}^2 g_{m2}^2 + V_{n5}^2 g_{m5}^2)/g_{m1}^2 + V_{n3}^2 (\frac{C_{gd1}}{C_{gd1} + C_{gs1} + C_p})^2 \quad (18)$$

where $V_{n2}$, $V_{n5}$ and $V_{n3}$ are input referred noise at the gate of $M_2$, $M_5$ and $M_3$ respectively.

The input referred voltage noise from $M_2$ and $M_5$ is scaled by the transconductance of $M_1$. Because $M_2$ and $M_1$ have similar biasing current, and NMOS normally has at least order of magnitude higher flicker noise coefficient than PMOS, the noise contribution from $M_2$ can not be neglected. To reduce the thermal noise from $M_2$, $g_{m2}$ has to be small, which leads to more voltage headroom for fixed biasing current. To reduce the flicker noise from $M_2$, the transistor has to be made big, which leads to stability problem that will be discussed in the next section. Therefore, it is also advantageous to bias $M_1$ in weak inversion and $M_2$ in strong inversion, so that the noise contribution from $M_2$ can be efficiently scaled down.

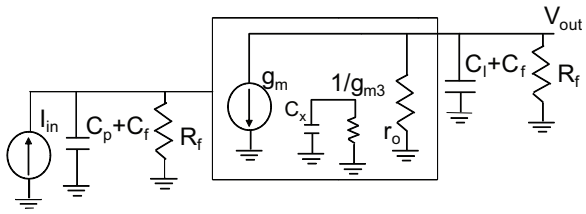


Fig. 4. Open circuit schematic after breaking the loop

The noise from $M_3$ is coupled through $C_{gd1}$ to the input of CSA. Since $M_1$ is normally very large, this component is not negligible. Considering the additional noise sources from (18), the optimization process has been modified, and the optimum point is slightly different.

## III. Stability analysis

The large input transistor makes the non-dominant pole of CSA amplifier closer to its dominant pole, thus the stability of CSA requires careful examination.

Assuming that the source follower is an ideal buffer and the reset MOS transistor has a very large equivalent resistance $R_f$, the small signal model of open loop circuit is shown in Figure 4. $g_{m3}$ is the transconductance of $M_3$, $r_o$ is the equivalent output resistance of CSA amplifier, $C_x = C_{gd1} + C_{db1} + C_{gd2} + C_{db2} + C_{gs3} + C_{sb3}$ is the total capacitance at the folding node and $C_l$ is the capacitance at the CSA output. The feedback network is $C_f$ in parallel with $R_f$. Thus, the loop gain can be derived as:

$$A(s)\beta = \frac{V_{out}(s)}{I_{in}(s)}\beta = \frac{g_m(r_o||R_f)(\frac{s}{Z_1}+1)}{(\frac{s}{P_1}+1)(\frac{s}{P_2}+1)(\frac{s}{P_3}+1)} \quad (19)$$

where zero is at $z_1 = 1/(R_f C_f)$ and poles are at $p_1 = 1/[R_f(C_f + C_p)]$, $p_2 = 1/[(r_o||R_f)(C_f + C_l)]$ and $p_3 = g_{m3}/C_x$. $p_1$ is attributed to the capacitive load at the input node, $p_2$ and $p_3$ are the two poles associated from CSA amplifier. The feed-forward zero comes from the RC network in feedback.

The pole and zero locations are shown in Figure 5. The unity frequency gain $f_u$ can be approximated as:

$$f_u = \frac{g_m C_f}{(C_f + C_l)(C_p + C_f)} \quad (20)$$

The first pole and zero occurs at relatively low frequency, their phase contribution can be approximately canceled. Therefore, the first non-dominant pole appears after $f_u$ is critical and ultimately determines the phase margin of the loop. It is reasonable to assume that the CSA amplifier's non-dominant pole is fixed, thus it is desired to place $f_u$ far away from $p_3$.

Smaller $C_f$ makes CSA more stable, however large amplifier gain is required due to high $C_p/C_f$ ratio. Thus, adding

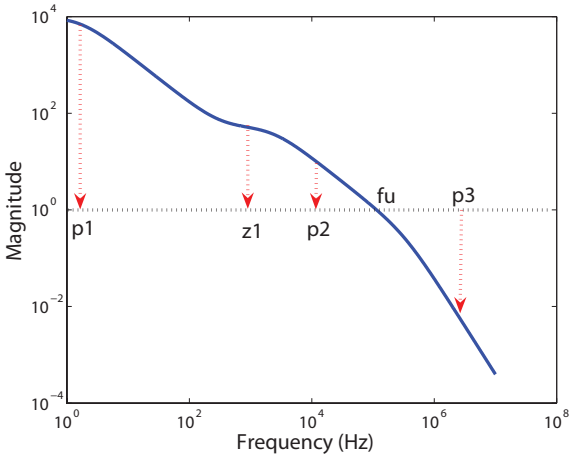


Fig. 5. Pole zero location of CSA

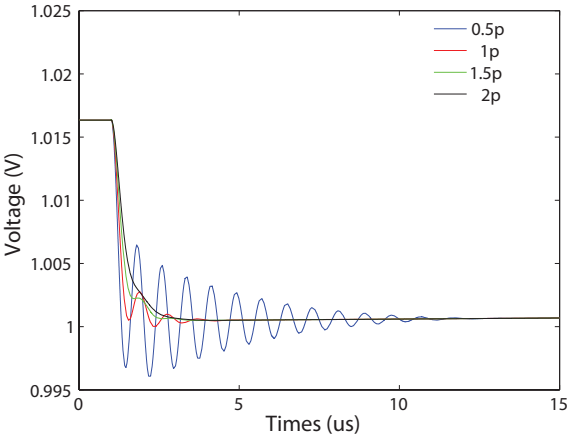


Fig. 6. Simulation of CSA with different compensation capacitors

compensation capacitive load $C_l$ is the only feasible option. For these reasons, for our design the chosen values for $C_l$ and $C_f$ are $2pF$ and $500fF$ respectively, and achieved phase margin is over $70^o$.

Figure 6 shows a simulation of the designed CSA with different compensation capacitors $C_l$. The effectiveness of previous stability model is proven. Though the added compensation capacitor slows down the circuit's step response to over $3us$, a large time constant of following shaper makes the overall readout system unaffected.

## IV. Results

The proposed system was implemented in $0.5\mu m$ CMOS technology. A microphoto of part of the designed chip is shown in Figure 7.

For characterization of the circuit without a sensor, a $0.5pF$ capacitor is connected serially to the input of the CSA. Capacitor enables controlled charge injection into the readout circuitry, as the current pulse at the input is generated by applying a known voltage step signal to capacitor. Figure 8 shows the measurement results of CSA. The input charge is swept from 3000 electrons to 90K electrons.

Fig. 7. Microphoto of implemented CSA

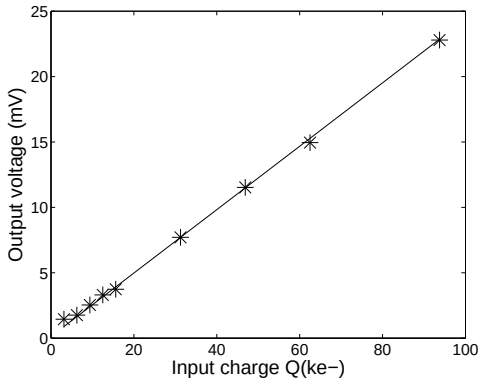


Fig. 8. Measured output voltage of CSA as a function of input charge.

## V. Conclusion

This work presents a design of a low-noise charge sensitive amplifier for radiation detection using semiconductor scintillator. Design challenges when facing large parasitic capacitance are discussed and analyzed. For optimization of the performance and increased sensitivity of readout circuitry, we have devised an optimization technique that incorporates accurate flicker noise model. Designed CSA achieves high sensitivity at low power consumption.

## VI. Acknowledgments

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