Noise and Interference Management in 3-D Integrated Wireless Systems

Emre Salman, Alex Doboli, and Milutin Stanacevic
Department of Electrical and Computer Engineering
Stony Brook University
Stony Brook, New York 11794
[emre, adoboli, milutin]@ece.sunysb.edu

***Abstract*—Three-dimensional (3-D) integration technology is an emerging candidate to alleviate the interconnect bottleneck by utilizing the third dimension. One of the important advantages of the 3-D technology is the capability to stack memory on top of the processor cores, significantly increasing the memory bandwidth. The application of 3-D integration to high performance processors, however, is limited by the thermal constraints since transferring the heat within a monolithic 3-D system is a challenging task. Alternatively, the application of 3-D integration to life sciences has not yet received much attention. Since typical applications in life sciences consume significantly less energy, the thermal constraints are relatively alleviated. Alternatively, interplane noise coupling emerges as a fundamental limitation in these highly heterogeneous 3-D systems. Various noise coupling paths in a heterogeneous 3-D system are investigated in this paper. Contrary to the general assumption, 3-D systems are shown to be highly susceptible to substrate noise coupling. The effects of through silicon vias (TSVs) on noise propagation are also discussed. Furthermore, design methodologies are proposed to efficiently analyze and reduce noise coupling in 3-D systems.**

I. INTRODUCTION

Advances in the electronics industry have long been driven by the continuous miniaturization of the integrated circuit (IC) technology. The scaling of the devices and interconnect has allowed higher integration levels, thereby improving the performance of a system while simultaneously reducing cost. This process, however, has recently slowed down due to device and circuit level limitations of conventional technology scaling.

Several emerging opportunities exist at different levels of abstraction to satisfy stringent design constraints in next generation integrated systems. At the technology level, three-dimensional (3-D) integration is a promising candidate to maintain the benefits of miniaturization by utilizing the vertical dimension rather than decreasing the size of the devices in two dimensions [1]. As depicted in Fig. 1, in a monolithic 3-D integrated circuit, multiple planes or tiers are stacked on top of each other where through silicon vias (TSVs) are utilized to achieve communication among the planes [2]. The advantages of 3-D integration technology include higher integration density and reduction in the length and number of the global interconnects. The application of 3-D integration technology to general purpose microprocessors has received significant attention in the past several years due to the opportunity to increase the memory bandwidth [3].

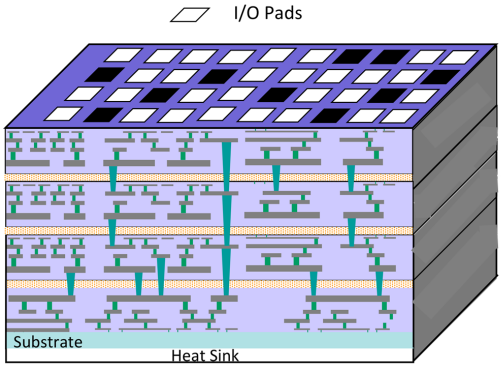

Fig. 1. **Monolithic 3-D integration technology where through silicon vias (TSVs) are utilized to achieve communication among the planes [2].**

One of the primary limitations of these multi-core processors utilizing 3-D integration technology is the temperature stability and the related cooling and packaging challenges [2]. Alternatively, the application of 3-D technology to life sciences has not yet received much attention. Since the power consumption of a typical biomedical system is significantly lower than a microprocessor, the thermal issues are relatively alleviated. Alternatively, the coexistence of different devices and circuit functionalities in a highly dense 3-D system requires stringent noise constraints.

The primary purpose of this paper is to explore the primary limitations related to noise coupling in highly heterogeneous 3-D systems with application to life sciences. The rest of the paper is organized as follows. The advantages of applying 3-D integration technology to life sciences are reviewed in Section II. Noise coupling among various planes in a 3-D system is discussed in Section III. Several methodologies are also proposed to efficiently analyze and reduce switching noise. Finally, the paper is concluded in Section IV.

II. APPLICATION OF 3-D INTEGRATION TECHNOLOGY TO LIFE SCIENCES

An important advantage of 3-D technology is the capability to achieve hybrid integration where diverse devices, technologies, and circuit functionalities can be combined in a monolithic system. An example of such a system is illustrated in Fig. 2 where an electrical plane is integrated with optical, mechanical, and bio-chemical planes. This op-

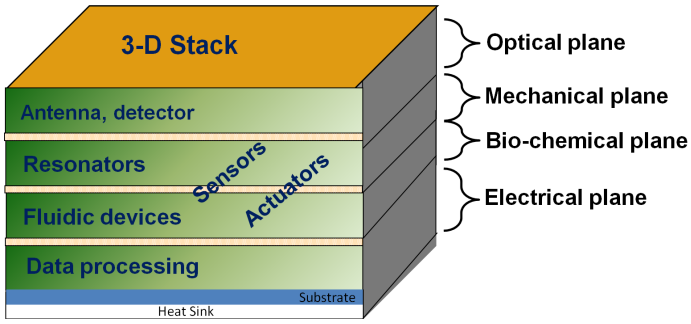

Fig. 2. **A highly heterogeneous 3-D system consisting of several planes with diverse functionalities.**

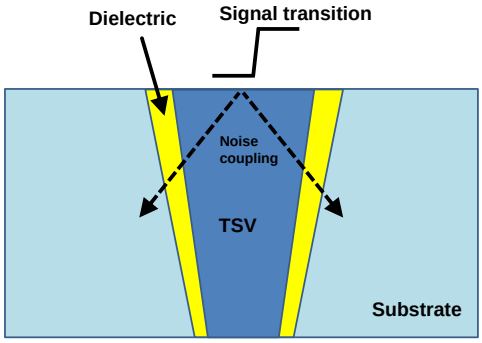

Fig. 3. **Cross section of a through silicon via carrying clock or data signals with high switching activity to illustrate noise injection into the substrate.**

portunity is particularly applicable to wireless communication circuits and systems in life sciences since the components and circuit blocks can be individually optimized based on the required functionality. For example, in a conventional transceiver circuitry, digital CMOS technology is preferred for data processing units due to higher noise margins and enhanced configurability whereas gallium arsenide based devices are preferred for the front-end blocks such as power amplifier, mixer, voltage controlled oscillator, and low noise amplifier. This communication circuitry can be integrated with a biomedical circuit consisting of, for example, ion-sensitive field effect transistors (ISFETs) [4].

Complex biomedical systems, such as implantable neural prosthesis and brain machine interfaces, require integration of power harvesting, telemetry, low-noise sensing, amplification and analog-to-digital conversion under severe constraints on size and power. 3-D integration provides attractive features for designing RF front-ends and power recovery circuits. The back metal layer can be RF-optimized, which includes metal thicknesses optimized for design of RF passives and tungsten gates shunts for reduced gate series resistance. The on-chip passives can be layout on the top tier, limiting their interference and area cost, as the interface circuitry would be layout in lower tiers. Similarly, the combination of CMOS technology with microfluidic systems provides new opportunities in the fields of biology and medicine [5]. Furthermore, power dissipation can also be significantly reduced by utilizing diverse materials such as leakage free phase change memory [6]. 3-D integration is a fundamental enabling technology that permits this heterogeneity required by life sciences and low power systems since multiple planes can be stacked within a monolithic system.

In such highly heterogeneous 3-D systems, noise coupling and interference among diverse blocks emerge as a significant limitation due to the requirement for sufficiently high signal-to-noise ratios. Alternatively, thermal issues are relatively alleviated since the applications in life sciences exhibit lower power density as compared to general purpose microprocessors. The application of 3-D integration technology to life sciences therefore requires significant research in the field of noise coupling and interference. Several noise coupling paths within a 3-D system are described in the following section.

III. Interplane Noise Coupling in a 3-D System

In a heterogeneous 2-D system where aggressor digital circuits are monolithically integrated with sensitive analog/RF circuits, noise coupling through the common substrate is a primary concern [7]–[9]. Increased digital operation concurrency, such as to optimize speed and power/energy consumption, typically produces high simultaneous switching noise. This noise is likely to propagate through the substrate and common power distribution network to the more sensitive analog blocks. By controlling the noise level, the performance of analog circuits is improved, for example at least 1-2 bits of resolution for a $\Delta\Sigma$ analog to digital converter operating at frequencies of about n x 100KHz to n x MHz.

It is typically assumed that a 3-D integrated system has enhanced noise coupling characteristics since each plane has a separate substrate, thereby improving signal isolation. This assumption, however, is a falsified representation of reality in practical 3-D systems due to two primary reasons:

- The through silicon vias (TSVs) carrying clock or data signals with high switching activity inject noise into the substrate of multiple planes, as shown in Fig. 3.
- Since multiple planes need to share a common power and ground distribution network due to limited number of pads, the simultaneous switching noise on the ground network propagates across the planes. Furthermore, the substrate of each plane is essentially interconnected since the substrate is biased by the ground network, as depicted in Fig. 4.

These two noise coupling mechanisms are described, respectively, in Sections III-A and III-B. Techniques to efficiently analyze and reduce switching noise are proposed, respectively, in Sections III-C and III-D.

A. TSV Related Noise Coupling

The first interplane noise coupling mechanism in 3-D systems is due to TSVs, as depicted in Fig. 3. A TSV consists of a metal such as copper or tungsten and a layer of

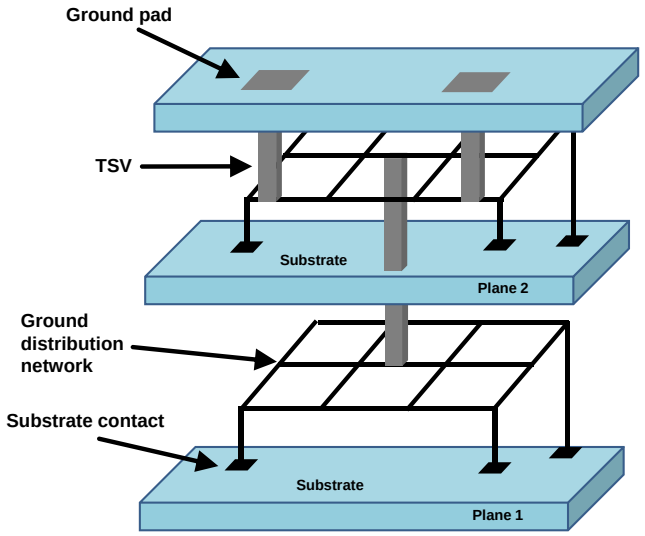

Fig. 4. **Common ground distribution network indirectly connects the substrate of the planes 1 and 2, degrading signal isolation among the planes.**

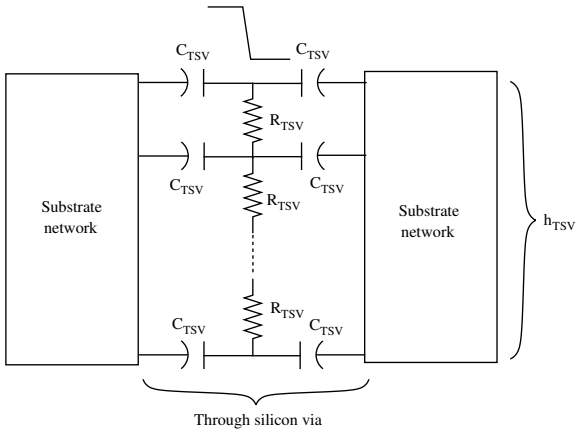

Fig. 5. **Circuit model to represent noise coupling into the substrate by a through silicon via.**

dielectric that surrounds the metal. The noise couples into the substrate when there is a fast signal transition within the TSV. Note that this coupling mechanism is similar to noise coupling into the substrate through source/drain junctions of a transistor since both coupling mechanisms are capacitive. The dielectric capacitance of a TSV, however, is significantly larger as compared to source/drain junction capacitance due to greater dielectric area. TSV related substrate noise coupling is therefore one of the primary noise injection mechanisms in 3-D systems. This coupling mechanism is modeled as shown in Fig. 5. The metal part of the TSV is represented as distributed resistance (R_{TSV}) whereas the dielectric is represented as distributed capacitance (C_{TSV}). Note that the noise injected into the substrate propagates throughout the substrate and may affect sensitive devices or may couple to other TSVs and propagate to neighboring planes.

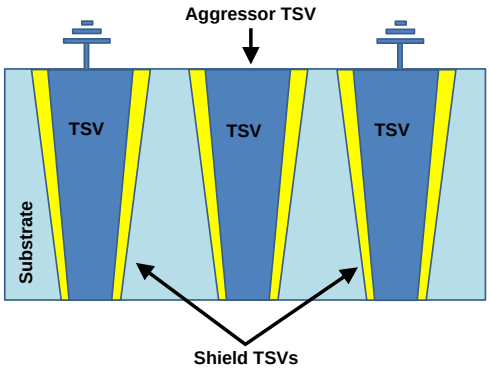

Fig. 6. **An aggressor TSV shielded by two TSVs that are connected to a sufficiently clean ground network to enhance noise isolation.**

The noise injected into the substrate by the TSV depends upon several physical parameters such as the height, width, and thickness of the TSV, thickness of the dielectric that surrounds the metal, and the distance of the aggressor TSV to the victim TSV or device. The height of the TSV is primarily determined by the substrate thickness. A shorter TSV is helpful to reduce the coupling noise by decreasing the coupling capacitance C_{TSV}. Increased dielectric thickness also reduces noise coupling due to reduced coupling capacitance. Alternatively, a higher dielectric thickness increases the overall area of the TSV, thereby reducing the integration density. The width and thickness of the TSV also affect noise injection by changing both the resistance R_{TSV} and capacitance C_{TSV} of the TSV. A wider and thicker TSV causes additional noise injection since the coupling capacitance is higher. The resistance is also reduced, further increasing the noise coupling.

Existing TSV placement methodologies primarily consider thermal stability and delay characteristics. Ignoring the effect of TSVs on the noise characteristics may significantly degrade the overall noise performance due to the noise injected into the substrate, as described in this section. Noise aware TSV placement methodologies should therefore be developed. For example, aggressor TSVs with high switching activity should be placed sufficiently far from the bulk node of the sensitive devices. These TSVs can also be shielded to further enhance noise isolation, as illustrated in Fig. 6. Note that the TSVs that behave as shield lines should be connected to a sufficiently clean ground or power network.

B. Ground Network and Substrate Related Noise Coupling

In typical 3-D integration technologies, the power/ground and signal pads are located at the top most plane, as shown in Fig. 4. Since multiple planes are stacked in a 3-D system, the number of required pads is generally higher. The overall number of pads that can be physically placed on a 3-D IC is, however, limited since the surface area of a 3-D IC is expected to be smaller as compared to a 2-D IC. Dedicated power/ground pads and networks are therefore not practical in a 3-D system due to limited surface area. Hence, to alleviate the constraint on the number of pads, several planes need to

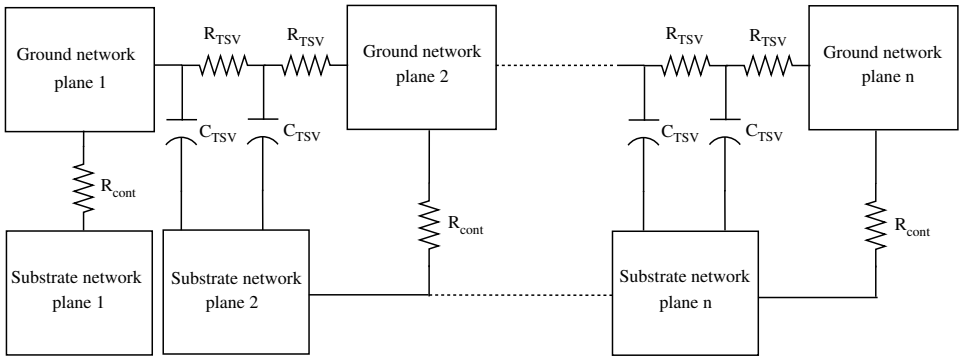

Fig. 7. **Circuit model to represent switching noise propagation among ground distribution networks, substrate, and TSVs.**

share a common power and ground distribution network.

As illustrated in Fig. 4, the ground networks of the planes 1 and 2 are connected with a through silicon via. Since the ground network of each plane is also connected to the corresponding substrate through the substrate contacts, the substrate of each plane is interconnected. Assuming an aggressor circuit is placed on plane 1, the switching noise propagates through the common ground network to plane 2. Furthermore, this noise can also be injected into the substrate of the second plane through the substrate contacts and TSV, thereby propagating towards more sensitive analog/RF circuits and sensors. A circuit model to represent this coupling mechanism is shown in Fig. 7 for n number of planes. The TSV model shown in Fig. 5 is used in this model to connect the ground networks located in different planes. Note that the number of stages used to model the TSV resistance and capacitance is equal to two. R_{cont} is the resistance of the substrate contact that connects the ground network with the corresponding substrate network. As illustrated in this figure, the substrates of different planes are interconnected both by the TSVs and the ground networks.

C. Efficient Noise Coupling Analysis

Fast analysis methods are needed to determine the robustness and sensitivity of the circuit to noise. Another advantage of fast noise analysis is the capability to evaluate various noise reduction techniques inside the system design loop.

Computationally efficient analysis of noise coupling is a challenging task in conventional 2-D ICs [10]–[12]. In a 3-D system, this issue is exacerbated due to the existence of multiple planes. As illustrated in Fig. 7, multiple networks need to be simultaneously considered in the analysis process. These networks include ground distribution and substrate network of each plane, and the TSVs that connect these networks into each other. Reasonable approximations are required to obtain a reduced order model for these networks while also satisfying the required accuracy.

Conventional extraction and analysis of a substrate network utilizes boundary element method (BEM) or finite difference method (FDM) which are not practical for 3-D systems due to significantly higher computational complexity. A methodology is described based on extracting only those regions of the substrate where there is significant current flow. The interaction between the ground and substrate networks is exploited to significantly reduce the computational complexity of the substrate extraction process. Specifically, small spatial voltage differences along the ground network are utilized to determine *voltage domains* on the substrate. Note these voltage domains on the substrate have approximately the same voltage. As illustrated in Fig. 8, these regions of the substrate are short-circuited by the ground network and therefore no major current flow exists in these domains. Since these regions are short-circuited, a coarse extraction is sufficient for these regions. This coarse extraction is achieved by reducing the number of substrate ports to only one. Note that a fine extraction is performed for those regions where there is significant current flow. This heterogeneous extraction of the substrate significantly reduces the computational complexity while maintaining a reasonable accuracy.

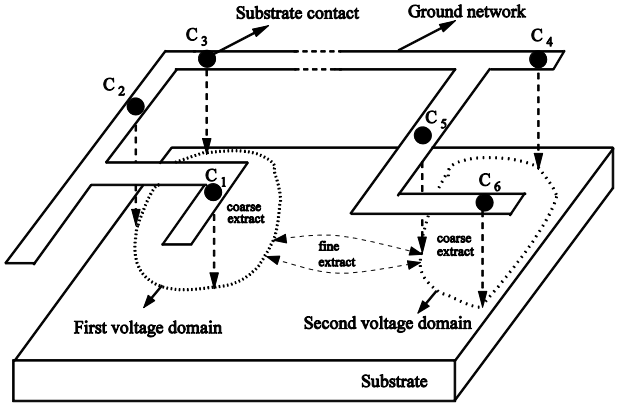

Fig. 8. **Identifying voltage domains on the substrate.** C_1**,** C_2**, and** C_3 **produce the first domain assuming** $V_{C1} \approx V_{C2} \approx V_{C3}$**. Similarly,** C_4**,** C_5**, and** C_6 **produce the second domain assuming** $V_{C4} \approx V_{C5} \approx V_{C6}$**.**

To evaluate the error in the estimated noise voltage and the improvement in computational complexity, the methodology is compared with a full extraction of the substrate achieved by Substrate-Noise-Analysis tool by Cadence [13]. An aggressor

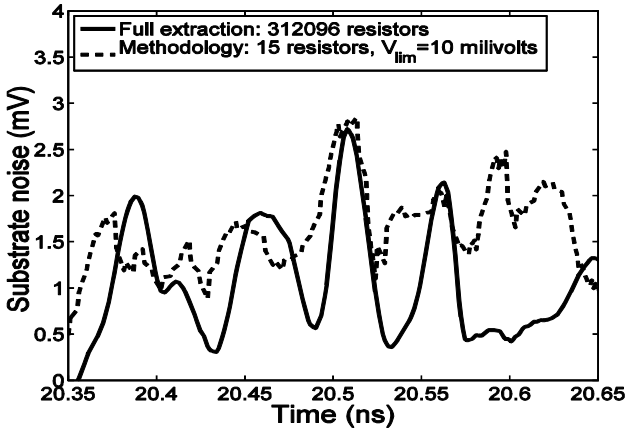

Fig. 9. **Comparison of the transient substrate noise at the victim node by simulating the fully extracted circuit and application of the methodology.**

digital core located close to a sensitive block in an industrial transceiver circuit with a bulk type substrate is used for the analysis. Full extraction of the substrate using Cadence tool produces 312,096 resistors and requires approximately six hours to complete. Alternatively, the proposed heterogeneous extraction methodology reduces the number of substrate resistances to 15 under the same computation environment, achieving more than four orders of magnitude reduction and requires negligible time to perform. The accuracy of the methodology in estimating the substrate noise voltage is shown in Fig. 9. As illustrated in this figure, the peak noise voltage is accurately estimated. The overall agreement between the two waveforms is also reasonable. Note that even though the error relatively increases at specific time instances, the methodology is significantly useful due to the computational efficiency. The effect of noise reduction techniques can be evaluated and the iterations between the design and analysis cycle can be achieved in a reasonable amount of time. The limitation of the methodology in terms of run time is the requirement to precharacterize each cell in the library for various input switching patterns and to perform a gate level simulation of the circuit to extract the required timing information.

D. Reducing Switching Noise

For complex 3-D mixed-signal designs, the system design flow must include noise management, *e.g.*, digital substrate noise, in addition to the more traditional constraints, like time and power/energy consumption. For example, in addition to new noise-aware synthesis techniques, noise management at the system level requires new methods for layout-aware modeling of digital and analog circuits, including their substrate and power nets.

A variety of different approaches exist to reduce switching noise or alleviate the effect of switching noise on sensitive circuits. These approaches can be classified under three primary categories [8]:

- To reduce the input noise magnitude of the circuit such as reducing the parasitic inductance or using separate power/ground networks for analog and digital circuits
- To modify the noise transfer medium such as utilizing guard rings or a higher resistivity substrate
- To reduce the sensitivity of the analog/RF circuit such as differential design

A methodology from the first category is described in this section to alleviate switching noise in a 3-D system.

Due to the complex interplane noise coupling paths, radical noise reduction techniques are required to satisfy signal integrity constraints in 3-D systems. One of the approaches to significantly reduce switching noise is to adopt an asynchronous design methodology [14]. Unlike synchronous systems, an asynchronous circuit does not have a periodic clock signal. The absence of a clock signal significantly reduces the noise spikes that occur at the primary and harmonics of the clock frequency. Alternatively, asynchronous circuits are typically not well supported by computer-aided design tools and the additional area required by the handshaking protocols may not always be justified [15]. Due to these reasons, asynchronous design methodologies have had limited acceptance in practical applications.

The methodology proposed in this section provides similar advantages as asynchronous circuits while still utilizing a synchronous circuit with a clock signal. Specifically, rather than having a periodic clock signal, a pseudo-random clock is utilized where the power spectral density (PSD) of the clock signal is spread over the frequency spectrum. Note that spread spectrum is a well studied topic in communication theory. In this work, a similar approach is applied to reduce noise in heterogeneous 3-D systems. The block level representation of the proposed methodology is shown in Fig. 10. A linear feedback shift register (LFSR) produces a pseudo-random number sequence. A probability adjustment block takes this pseudo-random number sequence as input to determine the amount of randomization. Next, the output of the probability adjustment block is used by the pseudo-random clock generator. This pseudo-random clock drives the aggressor circuitry rather than a standard periodic clock signal. Finally, the synchronizer unit synchronizes the data with the periodic clock.

As the randomization degree of the clock signal increases, the amount of noise reduction also increases since the PSD is further spread over the frequency spectrum. Alternatively, higher randomization produces a lower average clock frequency. In the proposed system, the probability adjustment block permits to determine the degree of the randomization. The appropriate randomization degree can be chosen based on the required noise reduction and minimum tolerable average frequency. This tradeoff between average frequency and reduction in noise is depicted in Fig. 11. Note that counter length is a parameter within the probability adjustment unit to determine the degree of randomization. The degree of randomization increases as the counter length is reduced, thereby achieving higher reduction in noise at the expense of reduced average clock frequency. Also note that even a sufficiently small degree of randomization can achieve a significant amount of reduction

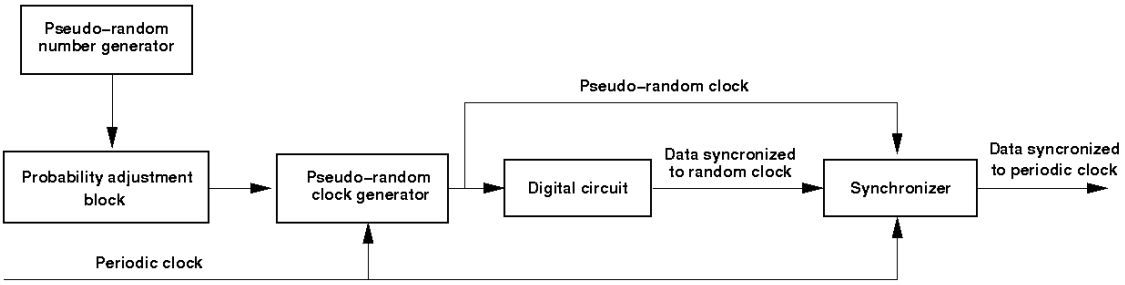

Fig. 10. **Pseudo-random clock generation to reduce switching noise and resynchronization with the periodic clock.**

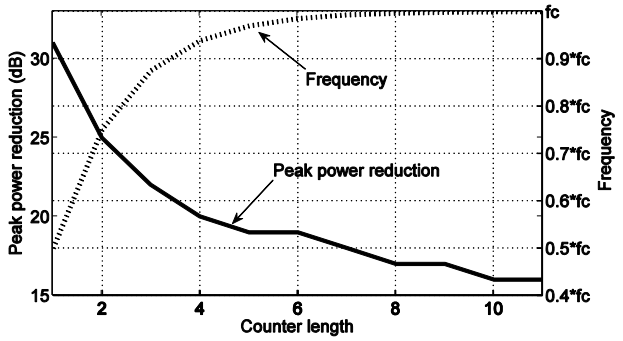

Fig. 11. **Tradeoff between the average frequency and reduction in noise.**

in noise. Specifically, for a counter length of 5, the frequency of the pseudo-random clock is 31/32 of the frequency of the periodic clock. The reduction in speed is less than 4% of the periodic clock while achieving approximately 18 dB reduction in the peak spectral power. This characteristic of the dependence is exploited to significantly reduce switching noise while maintaining the average clock frequency within a reasonable value.

IV. CONCLUSIONS

3-D integration is a promising technology not only for microprocessors, but also applications in life sciences due to the opportunity to integrate diverse devices. Noise and interference management of such a system emerges as an important challenge. Various interplane noise coupling paths have been identified in this paper. Simplified circuit level models for these coupling paths have also been provided. A methodology has been proposed to efficiently analyze noise coupling through the substrate of several planes within a 3-D system. A clock randomization methodology has also been described to reduce the spectral power of the switching noise by exploiting spread spectrum techniques from communication theory.

REFERENCES

[1] R. J. Gutmann *et al*., "Three-dimensional (3D) ICs: A technology platform for integrated systems and opportunities for new polymeric adhesives," *IEEE International Conference on Polymers and Adhesives in Microelectronics and Photonics*, pp. 173–180, October 2001.

[2] V. F. Pavlidis and E. G. Friedman, *Three-Dimensional Integrated Circuit Design*, Morgan Kaufmann, 2009.

[3] A. W. Topol *et al*., "Three-dimensional Integrated Circuits," *IBM Journal of Research and Development*, Vol. 50, No. 4/5, pp. 491–506, July/September 2006.

[4] B. Palan *et al*., "New ISFET Sensor Interface Circuit for Biomedical Applications," *Sensors and Actuators B*, Vol. 57, No. 1/3, pp. 63–68, September 1999.

[5] H. Lee, D. Ham, and R. M. Westervelt (editors), *CMOS Biotechnology*, Springer, 2007.

[6] S. Raoux *et al*., "Phase-Change Random Access Memory: A Scalable Technology," *IBM Journal of Research and Development*, Vol. 52, No. 4/5, pp. 465–479, July/September 2008.

[7] T. Kadoyama *et al*., "A Complete Single-chip GPS Receiver with 1.6-V 24-mW Radio in 0.18- μm CMOS," *IEEE Journal of Solid-State Circuits*, Vol. 39, No. 4, pp. 562–568, April 2004.

[8] A. Afzali-Kusha, M. Nagata, N. K. Verghese, and D. J. Allstot, "Substrate Noise Coupling in SoC Design: Modeling, Avoidance, and Validation," *Proceedings of the IEEE*, Vol. 94, No. 12, pp. 2109–2138, December 2006.

[9] D. K. Su, M. J. Loinaz, S. Masui, and B. A. Wooley, "Experimental Results and Modeling Techniques for Substrate Noise in Mixed-Signal Integrated Circuits," *IEEE Journal of Solid-State Circuits*, Vol. 28, No. 4, pp. 420–430, April 1993.

[10] B. R. Stanisic, N. K. Verghese, R. A. Rutenbar, R. Carley, and D. J. Allstot, "Addressing Substrate Coupling in Mixed-Mode IC's: Simulation and Power Distribution Synthesis," *IEEE Journal of Solid-State Circuits*, Vol. 29, No. 3, pp. 226–238, March 1994.

[11] R. Gharpurey and R. G. Meyer, "Modeling and Analysis of Substrate Coupling in Integrated Circuits," *IEEE Journal of Solid-State Circuits*, Vol. 31, No. 3, pp. 344–352, March 1996.

[12] J. P. Costa, M. Chou, and L. M. Silveria, "Efficient Techniques for Accurate Modeling and Simulation of Substrate Coupling in Mixed-Signal IC's," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 18, No. 5, pp. 597–607, May 1999.

[13] "Assura RCX^{TM}, SubstrateStorm^{TM}, Spectre^{TM} tools," [Online]. Available: http://www.cadence.com.

[14] C. H. Van Berkel, M. B. Josephs, and S. M. Nowick, "Scanning the Technology Applications of Asynchronous Circuits," *Proceedings of the IEEE*, Vol. 87, No. 2, pp. 223–233, February 1999.

[15] J. Sparso, *Asynchronous Circuit Design: A Tutorial*, Technical University of Denmark, 2006.