Extended Counting ADC for 32-channel Neural Recording Headstage for Small Animals

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***Abstract*— Extended counting analog-to-digital converter (ECADC) combines the accuracy of delta-sigma modulation and the speed of algorithmic conversion. This conversion architecture is shown to be useful in biomedical applications, where both resolution and speed are demanded. This work presents a design of ECADC for 32 neural recording channels. Several power optimizing methods are described. The designed converter achieves a resolution of 13 bits and a sampling frequency of 512 kHz. With 3.3V supply, the total power consumption is estimated to be 7 mW. The whole system including 32 neural recording channels is fitted in an area of 3mm $\times$ 3mm in 0.5μm CMOS process.**

I. Introduction

The ability to record many channel neuronal data from behaving animals is critical to efforts to understand the function and dysfunction of neural circuits in the intact brain. The success in fabrication of MEMS structures for microelectrode arrays is mitigated by the limitation of the current acquisition, signal processing and communication methodologies. Recording systems that would enable acquisition of neural signals and communicate gathered information to recording station in such a way that small animal movement is restricted in minimal way are still not available due to size and weight constraints.

Existing systems for multi-channel recording mainly use analog headstage requiring a number of wires equal to the number of channels, leading to restriction of movement and poor scalability. Most of these systems use pre-amplifier and front-end filtering to improve the signal-to-noise ratio before transmission to a remote data logger. Wireless transmitting devices might solve that problem, but current generations based on analog multiplexing also scale poorly and are susceptible to noise. The design of a headstage with on-chip analog-to-digital conversion would enable digital telemetry of neural signals in their entirety and provide a high-throughput recording systems that can assist neuroscientists to configure data collection mechanism for reliable data logging [1].

The main constraint in the design of proposed multi-channel system is power and size of analog-to-digital converters. We propose the use of extended counting technique, that represents combination of incremental and algorithmic ADC, providing resolution of the interest, and on the other hand small form factor. Delta-sigma modulation achieves a high resolution by means of oversampling. This normally leads to an increased power consumption. Moreover, these implementations require digital decimation filters that may occupy several square millimeters of silicon area [2]. Algorithmic ADC [3], [4] has much smaller power consumption and can operated at higher speed. However, the linearity is limited by component matching. In standard CMOS process, only 8-10 bits of resolution can be achieved. Extended counting converter combines the advantages of delta-sigma modulation and algorithmic A/D conversion [2], [5]-[8]. It achieves a good trade-off between accuracy and speed, thus is a good selection for the neural recording system. This paper presents a design of extending counting ADC for 32-channel neural recording system with novel solutions regarding power consumption and size reduction.

II. Design of Extended Counting Converter

The proposed headstage requires a resolution of 13-bits and sampling rate of 32 kHz per channel to record neural signals in small animals. The size constraint leads to channel multiplexing and increased data rate of converter. Under the specifications stated above, extended counting is chosen as the architecture of our ADC.

The extended counting conversion contains two conversion modes. The converter passes two modes one after the other in time, and each mode needs several clock cycles to complete. Hence, one sample is converted through several clock cycles. A block diagram of the architecture is shown in Figure 1. The first mode, which is called "counting conversion", is a resettable first-order delta-sigma modulator. It converts the most significant bits (MSB). Then the residue of the first mode, V_{count}, is fed into the second mode, called "extended counting conversion", which is generally implemented as an algorithmic conversion. The least significant bits (LSB) are obtained in the second mode.

For the designed ADC, we acquired 3 bits from the counting stage and 10 bits from the extended counting stage. So, we assigned 8 clock cycles to the first stage, and 6 clock cycles to the second stage to ensure that the component mismatches limit the LSB resolution to 10 bits. Two additional clock cycles

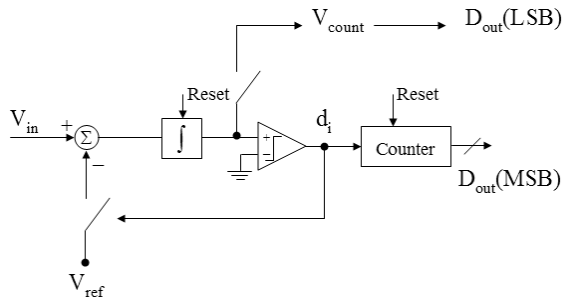

Fig. 1. Block diagram of extended counting converter

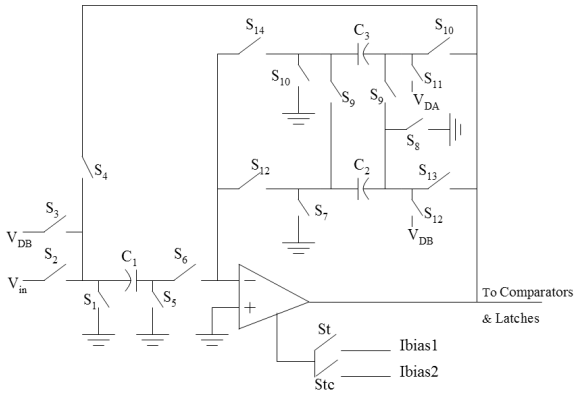

Fig. 2. Single-ended schematic

are required in the transition between stages, leading to a total 16 clock cycles needed for one conversion.

Figure 2 shows a single-ended schematic of the designed ADC. The implemented fully differential structure is not shown here for simplicity. Compared with the reported architecture [2], three capacitors are used instead of four. All capacitors are nominally equal, and C_2 and C_3 are connected together in the first stage to provide the larger feedback capacitor. This structure results in better power and area performances. However, an additional half clock cycle is required. Thus the clock frequency is set to 8.4MHz. Figure 3 shows the clock scheme of one conversion.

The designed switched capacitor implementation of ECADC is described. An initial reset is performed before each conversion. Each step includes two phases. In the first phase, the input voltage V_{in} is sampled and the output of opamp is held constant for the comparator to decide the digital output bits D_{out}. In the second phase, a reference voltage V_{DB} depending on the sign of D_{out} from last phase is fed back to the input. Therefore a first-order delta-sigma modulation is performed. The same building blocks are used. Similar circuit operations take place in the extended counting stage, except that a separate reference voltage V_{DA} is used to generate two digital bits in one clock cycle. For better linearity, an amplification with the factor of 2 is performed to initialize the second stage [2].

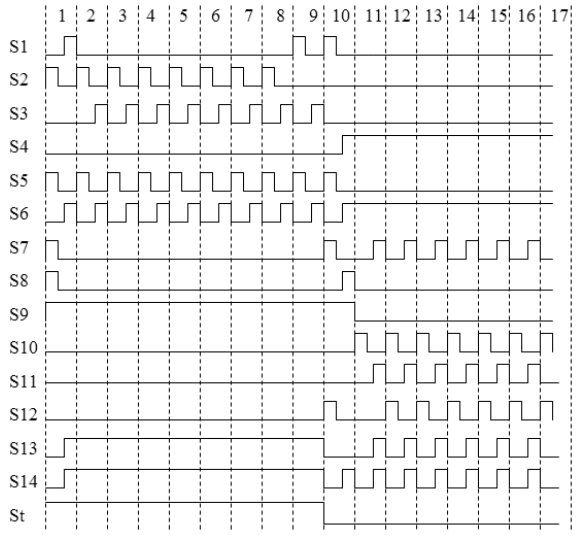

Fig. 3. Timing diagram

A. Optimizing the Number of ADC

The power consumption of ADC is mainly determined by the sampling speed, and the sampling speed is limited by the settling time of OPAMP used in the ADC. To minimize core size, only one ADC is usually chosen. Signals from 32 channels are multiplexed before fed into the ADC. However, this results in a high sampling frequency ADC, which leads to increased power consumption. To achieve an optimum point between size and power, a detail analysis is required.

The settling time is controlled by two parts: slew rate (SR) and gain bandwidth (GBW) of the OPAMP. If one third of the settling time is assigned to slew rate [9], and a single-pole model of OPAMP is used, two equations can be derived:

$$I_D = 3 \cdot f \cdot V_{pp,diff} \cdot C_{L,eff} \tag{1}$$

$$I_D \cdot \frac{W}{L} = \frac{9ln^2 2}{2\mu_0 C_{ox}} \cdot (N+1)^2 f^2 \cdot (\frac{C_{L,eff}}{m})^2 \tag{2}$$

where f is the sampling frequency, I_D is the drain current of the OPAMP input differential pair, $V_{pp,diff}$ is the largest differential full scale slewing, $C_{L,eff}$ is the effective load presented at the output of the OPAMP, N is the resolution, and m is the feedback factor. The first equation gives the SR limited current requirement, and the second equation gives the GBW limited current requirement. It is clear that when the SR limitation is dominant, the drain current is linear with frequency, when the GBW limitation is dominant, the drain current follows a square law. Hence, the optimum point between size and power lies when the biasing current of OPAMP is selected at the SR limited region, but as close as to the GBW limited region.

With the design process parameters and the unit capacitance used in our design, MATLAB simulations are performed to find the optimum number of ADCs. Figure 4 plots the current consumption of the OPAMP as a function of sampling frequency f.

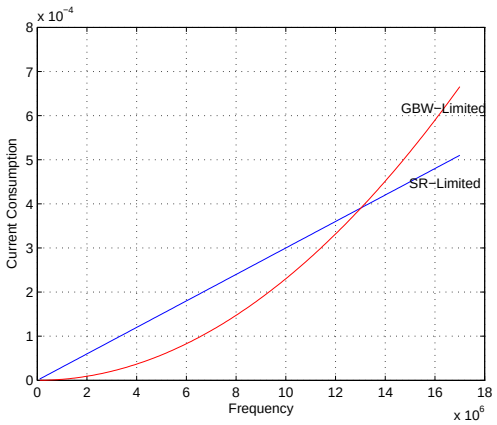

Fig. 4. Current consumption versus clock frequency

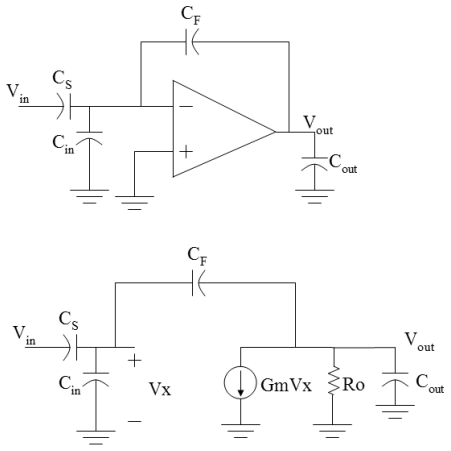

Fig. 5. Typical circuit scheme in ECADC and its equivalent small signal model

B. Different Settling Behaviors in Two Stages

Figure 5 shows a typical circuit scheme in ECADC architecture and its equivalent small signal model. Assuming the output impedance of OPAMP R_o is very large and the input parasitic capacitance C_{in} is small, a small-signal analysis indicates that the transfer function is:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{C_S(sC_F - G_m)}{C_F G_m + s(C_{out}C_S + C_F C_S + C_F C_{out})} \quad (3)$$

Assuming the input voltage is a unit step, the voltage step in both time and frequency domain is

$$V_{in}(t) = U(t), V_{in}(s) = 1/s. \quad (4)$$

Thus the output voltage in both domain is

$$V_{out}(t) = \frac{C_S}{C_F}U(t) - \frac{C_S}{C_F}[1 + \frac{b}{a}]e^{-bt}U(t), \quad (5)$$

$$V_{out}(s) = \frac{1}{s}\frac{C_S(sC_F - G_m)}{C_F G_m + s(C_{out}C_S + C_F C_S + C_F C_{out})}, \quad (6)$$

where

$$a = \frac{G_m}{C_F}, b = \frac{G_m C_F}{C_{out}C_S + C_F C_S + C_F C_{out}}. \quad (7)$$

The time constant τ of the output voltage is then derived to be

$$\tau = \frac{1}{b} = \frac{C_{out}C_S + C_F C_S + C_F C_{out}}{G_m C_F}. \quad (8)$$

Figure 6 shows a simulation result of OPAMP outputs in one conversion. The solid line is the positive output of OPAMP, and the dashed line is the negative output of OPAMP. The fastest settling happens in the first few clock cycles, where the converter works in counting stage. In this stage, C_S=1p, C_F=2p, C_{out} equals to the parasitic output capacitance of OPAMP. In the last few clock cycles, the converter works in extended counting stage, where C_S=1p, C_F=1p, C_{out} equals

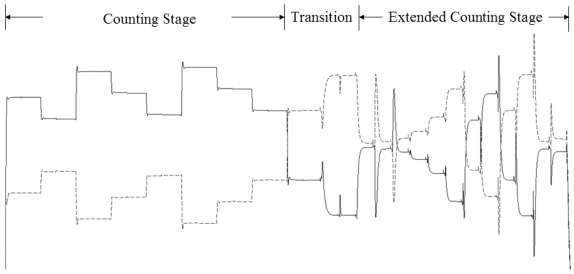

Fig. 6. Different settling behaviors

to 1p plus the parasitic output capacitance of OPAMP. In the transition between stages, where the amplification required to initialize extended counting stage is performed, C_S=2p, C_F=1p, C_{out} equals to the parasitic output capacitance of OPAMP. If the output parasitic capacitance of OPAMP is assumed to be 300f, then

$$\tau_{counting} = \frac{1.45}{G_m}, \tau_{extended} = \frac{3.6}{G_m}, \tau_{transition} = \frac{2.9}{G_m}. \quad (9)$$

From the above equation, the settling time in extended counting stage is almost 2.5 times than that in counting stage, and the time constant in extended counting stage and transition are fairly the same. Thus, the small-signal analysis does a good prediction of the circuit behavior, and the calculation results approximately match the simulation. Therefore, it is clear that power is wasted if the same OPAMP is used in the whole conversion.

Two methods are developed to combat this problem. Firstly, different clocks can be used in conversion. Shorter time period can be assigned to counting stage to take advantage of its shorter time constant. Hence, faster speed can be achieved while consuming the same amount of power, or in other word, lower power is consumed while maintaining the same conversion speed.

Instead of using clocks with different periods, we implemented a reconfigurable OPAMP with adjustable biasing cur-

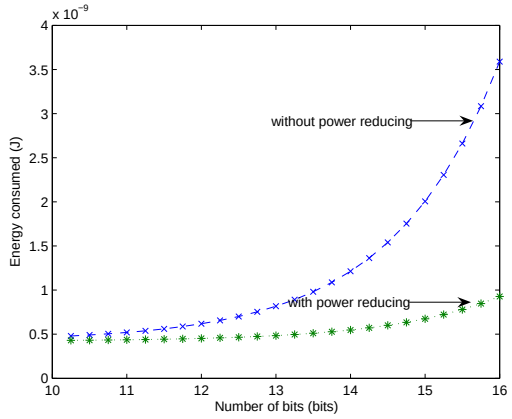

Fig. 7. Power reduction versus number of bits

TABLE I
SUMMARY OF ADC.

Resolution	13 bit
Supply Voltage	3.3V
Clock Frequency	8.4MHz
Sample-frequency	512KHz
Power Consumption	7mW
Input Range	$\pm$1V
Core area	0.7mm by 0.8mm

rent. Smaller biasing current is needed when the time constant is lower. Hence, the OPAMP is switched to a higher biasing when counting stage is finished. It is a similar concept described in [10]. In figure 2, $Ibias1$ and $Ibias2$ are two different biasing currents for counting stage and extended counting stage, respectively. In figure 3, St is the clock controlling biasing current of OPAMP, and Stc is a complementary clock of St. The switching is performed in the first phase of 10th clock, when the OPAMP is not operating. Thus, additional clock cycle penalty is avoided to reconfigure the OPAMP.

Since G_m^2 is proportional with the drain current of OPAMP, and 8 clock cycles from counting stage can benefit from this technique, the total power reduction is about 40% for our design. If more bits resolution are required from counting stage, the reduction is even greater. Using the same conditions as above, and assume 10 bits resolution is provided from extended counting stage, the power consumed in one conversion with two different structures is plotted in Figure 7.

III. SIMULATION RESULTS

The designed ADC was simulated using Cadence SpectreS simulator and BSIM3 version 3.1 transistor models. Figure 8 shows the simulated integral nonlinearity(INL) of ADC. The x-axis is the input voltage, swept from 1.2V to 2.1V, with a step size of 50 mV. The Y-axis is the corresponding INL in unit of 1 LSB at 13 bit. TableI presents the performance summary of the designed ADC.

IV. CONCLUSION

This work presents a design of extended counting analog-to-digital converter (ECADC) incorporated in a neural recording

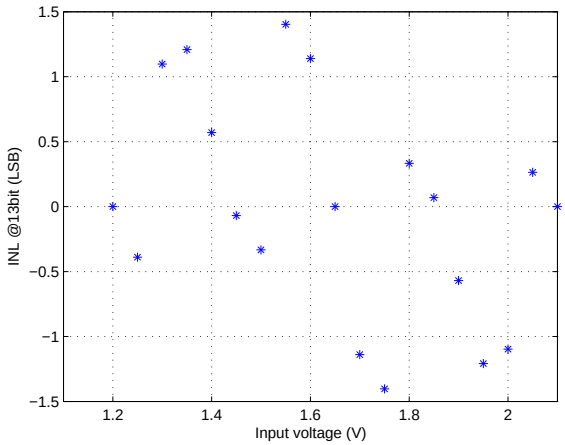

Fig. 8. *Integral nonlinearity(INL) of ADC.*

system. Several design issues regarding power consumption and size are proposed. An interesting technique that reduces power consumption by about 40% is developed. The preliminary prototype of the 32-channel neuro digitizer chip is implemented using 0.5μm CMOS technology and its functionality will be fully verified with in-vitro testing.

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