Design of Mixed-Signal Circuits for Wireless Communication Systems and Implanted Neural Devices in 3D Technology

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The three-dimensional (3D) integrated circuit technology developed by MIT Lincoln Laboratory allows circuit structure that forms on several silicon-on-insulator (SOI) substrates to be integrated into a 3D integrated circuit. This 3D technology gives the possibility of better thermal and noise management, more compact design, and so on. However, circuit design in the 3D technology has not been fully understood. The design methodology should also be developed in order to capture all the design issue.

Continuous-time ΔΣ modulators are widely used in wireless communication systems due to their power efficiency, superior linearity at low bandwidths, and inherent bandwidth resolution tradeoff in the noise-shaping characteristic. The designed modulator is a fifth order reconfigurable continuous-time ΔΣ modulator for UMTS, WCDMA, and GSM wireless communication standards. The modulator topology is optimized for the design complexity, robustness, and power consumption. The design specification of each building block of the modulator is fully specified. As the building blocks are designed and layed out in the 3D technology, the design issues of the 3D integration process will be explored and studied. In order to have a better understanding of the technology, some basic building blocks are designed before designing the entire system. First, two Gm-C integrators were implemented. The CMOS transistors of the two integrators are equally sized. The only differences are the values for the source degenerated resistor and the load capacitor. By this way, some design tradeoffs, like the tradeoff between the gain and the bandwidth of the integrator, can be simulated and measured. Then, the reconfigurable modulator is designed and the design methodology is developed.

Implantable neural prosthesis and brain machine interfaces require integration of power harvesting, telemetry, low-noise sensing, amplification and analog-to-digital conversion under severe constraints on size and power. 3D technology offers considerable advantages in realizing such complex systems by reducing interference and providing dense interconnections. Additionally, FD-SOI technology has good properties of parasitic capacitance reduction, smaller leakage current and high noise immunity from on-chip digital circuitry. These advantages enable designs in SOI technology with lower power consumption, smaller area and better noise efficiency than designs in conventional bulk CMOS technology. We implemented power harvesting through inductive coupling link, with the on-chip inductor, designed in back RF metal layer, that occupies the whole 2D area of the chip. Designed low-noise voltage preamplifier and current measuring analog-to-digital converter for recording of neuro potentials and neurochemical signals demonstrate better power and noise performance than the designs in bulk technologies.

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