Low-Power Low-Noise Neural Amplifier in 0.18 μm FD-SOI Technology

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Abstract— **For recording of neural signals from large population of neurons, stringent constraints are imposed on the design of neural amplifiers. We have designed neural amplifier in FD-SOI technology in order to achieve lower power consumption, smaller area and better noise efficiency factor compared to the standard bulk processes. A symmetric pseudo resistor was realized with resistances on the order of 10$^{15}\Omega$, enabling a low cut-off frequency of 0.6 mHz. The designed neural amplifier occupies area of $0.004mm^2$, with simulated performance demonstrating a noise level of 3.07 μV at power consumption level of 6 μW.**

I. Introduction

The development of a direct neural interface with the central and/or peripheral nervous system has been a goal of the neuroscience and biomedical engineering communities for many decades. The knowledge gained from neural recording is one of main requirements to both fundamental research in how spatial population of somatosensory neurons encode mechanical stimuli (which occur during touch, joint movements, and muscle constrictions) and the engineering feedback-controlled functional electrical stimulation (FES) of muscles used in locomotion for paralysis victims [1], [2].

The most critical block in neural recording system is low-power low-noise neural amplifier which is in the most front of the system. There have been considerable research efforts in design of low-power low-noise neural amplifiers in recent years in bulk CMOS processes [3], [4], [5], [6], [7]. MOS-bipolar pseudoresistor element was used to achieve very low cut-off frequency in these design.

To achieve lower power consumption, smaller area and better noise efficiency factor, FD-SOI process [9], was used for design of the amplifier. FD-SOI process has good properties of parasitic capacitance reduction due to dielectric reduction, smaller leakage current, and high noise immunity from on-chip digital circuitry [10], [11]. Since the conventional bulk CMOS technology has the serious drawback of high leakage current as the transistor feature size is scaled down, design in bulk CMOS technology would meet an unavoidable problem in terms of power and noise, which are the most important metrics for neural amplifier design. As the design of neural recording system targets to implement fully implantable chip with integrated power harvesting and telemetry, neural amplifiers and analog-to-digital converters, integration of such a system in 3D technology could offer considerable advantages.

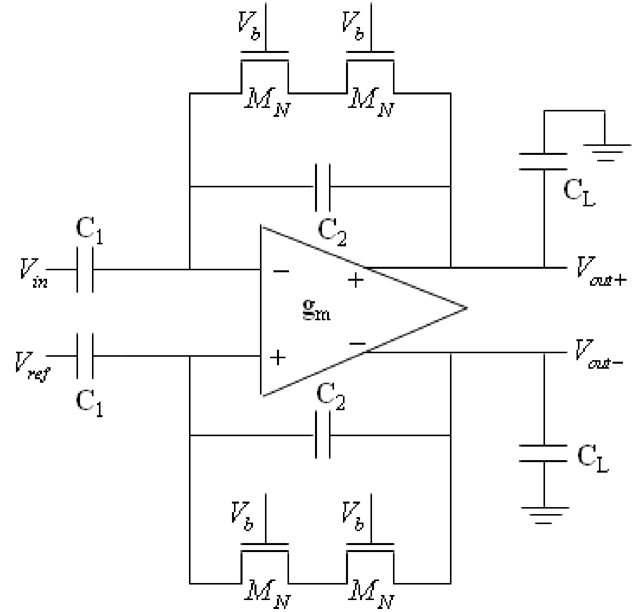

Fig. 1. *Schematic of fully differential neural amplifier in MITLL 0.18 μm FD-SOI Process.*

Different functional blocks of the systems could be designed in different vertical tiers, reducing significantly the overall area and decreasing the effects of interconnections. For example, large inductor needed for power harvesting in inductive coupling link could be designed in back RF metal layer and could be occupy the whole 2D area of the chip on that metal level.

We designed low-power, high noise-efficiency-factor (NEF) neural recording amplifier having a fully differential structure to minimize the effects from digital circuitry and fully symmetric MOS resistor element. Finally, simulation results are presented.

II. Neural Amplifier Design

Figure 1 shows the schematic of amplifier design. The whole structure of the neural amplifier is similar to previous design [4] so that the midband gain A_M is set by C_1/C_2, and the bandwidth is g_m/A_MC_L, where g_m is the transconductance of the operational transconductance amplifier (OTA).

A. Symmetrical MOS resistor element

The cut-off frequency of DC rejecting high-pass filter has to be set at very low value, in mHz range, due to frequency content of the neural signal. To avoid using large off-chip capacitance, large on-chip resistor is needed. Using MOS transistor operating in subthreshold region of operation as a high-resistive element was first proposed in [8]. In [3], MOS-bipolar devices acting as pseudoresistors are used to create such a high floating resistances of the range from $10^{11}\Omega$ to $10^{14}\Omega$. However, the diode-connected PMOS devices give unsymmetrical resistance. For the negative V_{GS} voltage, device behaves as diode connected PMOS transistor, while for the positive V_{GS}, it behaves as parasitic p-n-p bipolar transistor. The resistance will depend on the sign of voltage across the resistor. This causes dependance of the cut-off frequency of the high-pass filter on the input signal and introduces distortion of the output signal. The value of the resistance is not controlled.

In FD-SOI process, MOS transistor operating in subthreshold can provide higher resistance than in bulk process and also a symmetrical one with respect to sign of the voltage across it. If the gate voltage is much lower than drain and source voltage for NMOS transistor, 300 mV lower for minimum size square transistor, the equivalent circuit represents two back-to-back diodes between source and drain. Figure 2 shows the simulated current-voltage characteristic of NMOS transistor, with size of 0.6μm $\times$ 0.6μm, with the gate voltage fixed at 0.2 V and voltage across the pseudo-resistor varied from -200 mV to 200 mV, with the common-mode value set at 750 mV. The equivalent resistance will be on the order of $10^{15}\Omega$ for region of almost 200 mV and is not dependent on the gate voltage. If the gate voltage is reduced further, the transistor will behave as transistor in subthreshold region with the body-effect coefficient being almost equal to one in the bulk-process, as the body is not fully depleted until gate voltage is lower than source-drain voltage. Figure 3 shows the simulated current-voltage characteristic of NMOS transistor for this case with the gate voltage fixed at 0.6 V. The dependence of the equivalent resistance on the biasing voltage V_b of the NMOS element (M_P in Figure 1) is shown in Figure 4.

To reduce the distortion due to large output signals two series connected pseudo MOS elements can be used so that the total time constant is set to $2R_MC_2$, where R_M refers to resistance of pseudo MOS element. Therefore, the low cut-off frequency of neural amplifier is determined by $1/(2\pi 2R_MC_2)$.

B. Low-Noise Low-Power OTA design

Since FD-SOI devices offer near-ideal body effect coefficient of unity (1.6 for bulk CMOS device), it is expected to have 30-40 percent higher saturation drain current in a FD-SOI device than in a bulk device with similar parameters [10]. This makes possible to achieve the same performance at lower power level.

Figure 5 presents the schematic of operational transconductance amplifier (OTA) [3]. Basic circuit structure is a current mirror OTA with two cascode transistors for each output. Since there is no noise contribution for adding cascode transistors

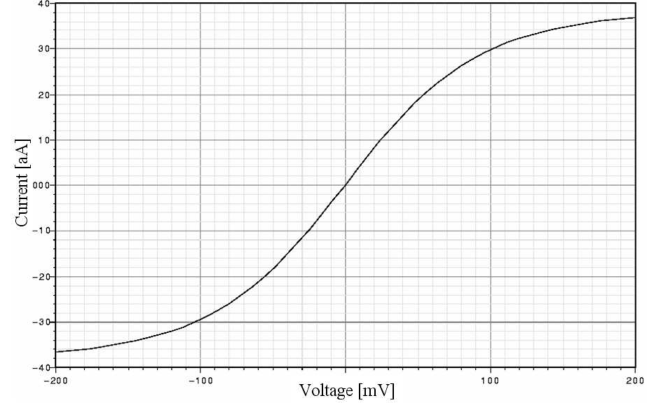

Fig. 2. *Simulated current-voltage relationship of NMOS element (M_N in Figure 1) for voltage Vb set at 0.2 V.*

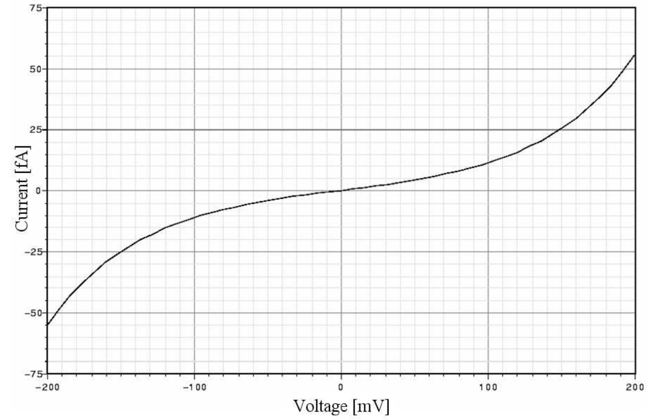

Fig. 3. *Simulated current-voltage relationship of NMOS element (M_N in Figure 1) for voltage Vb set at 0.6 V.*

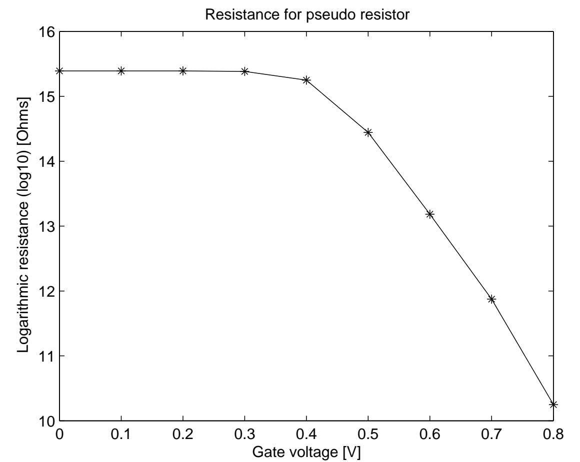

Fig. 4. *Equivalent resistance of NMOS element as function of gate voltage Vb).*

they can be used for increasing OTA gain without affecting the performance. Also, the output voltage swing is limited by the linear range of the high-resistive element, not by the cascode transistors. The main trade-offs in the OTA design are occurred among noise, power, and stability. If we only consider the power consumption, the maximum performance may be obtained when the value of the transconductance/drain current ratio (g_m/I_d) is the largest. However, the input referred thermal noise of OTA is given as

$$\overline{v_{in,thermal}^2} = \frac{16kT}{3g_{m1}}[1 + \frac{g_{m3}}{g_{m1}} + \frac{\frac{g_{m3}^2}{g_{m5}}}{g_{m1}} + \frac{g_{m7}\frac{g_{m3}^2}{g_{m5}^2}}{g_{m1}}] \quad (1)$$

g_m/I_d ratio and size of transistors should be considered to minimize input referred thermal noise contribution. As total power consumption is determined by biasing current, we have chosen a lower biasing current. From the noise analysis, input transistors M_1 and M_2 should be sized with as large W/L ratio as possible so that it gives a maximum g_m/I_d ratio. In the same manner, the noise contribution of transistors M_3 through to M_7 can be minimized by choosing small W/L ratio or minimizing g_m/I_d ratio. Increasing the length of these transistors gives rise to parasitic capacitances, causing second pole of OTA to move closer to dominant pole created by load capacitor C_L and reduces phase margin. This effect is reduced in FD-SOI process, since the parasitic capacitance is smaller than in bulk process and larger phase margin is obtained. Further minimizing of noise contribution can be carried out by sizing transistors M_5 and M_6 properly so as to make higher g_{m5}/I_d ratio than g_{m3}/I_d ratio. Effect of flicker or $1/f$ noise is minimized by choosing input pMOS transistors and by increasing the gate area of transistors in the design. The input transistors M_1 and M_2 are designed as H-gate transistors with separate source bulk connection to improve the matching between them at expense of increased area. The sizes of all transistor in OTA and their respective g_m/I_d ratios are given in Table 1.

Device	W/L(μm)	I_d(μA)	$g_m/I_d(V^{-1})$
$M_{1,2}$	210/0.5	1	34.08
$M_{3,4}$	0.6/9.6	1	5.22
$M_{5,6}$	1/9.6	1	7.14
$M_{7,8}$	1.6/6	1	4.62
$M_{9,10}$	3.2/0.8	1	11.33
$M_{11,12}$	1.6/0.8	1	24.86
$M_{13,14}$	8/4	2	8.33

Table 1: *Transistor sizes and their respective g_m/I_d ratios.*

C. Common mode feedback circuit

For the implementation of common-mode feedback circuit, we have chosen continuous-time circuit shown in Figure 6. The common-mode output voltage is set to $V_{DD}/2$, 0.75 V. If the output common-mode level increases, current of M_{15} and M_{18} will increase and the current of $M_{16,17}$ will decrease. This causes increment in V_{CMFB} and makes the V_{SG} of $M_{7,8}$ decrease, followed by decrease in common-mode output voltage.

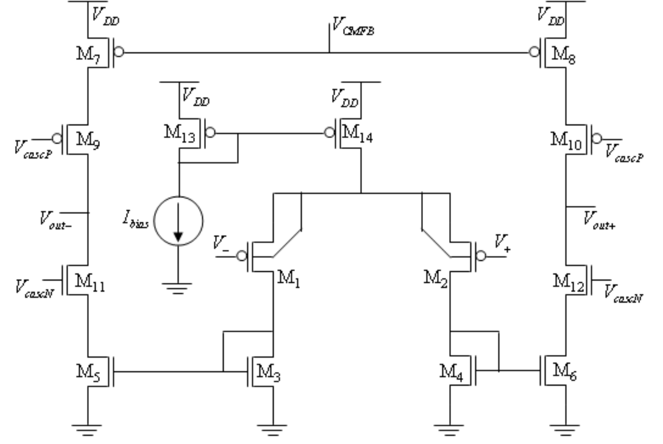

Fig. 5. *Schematic of operational transconductance amplifier used in low noise amplifier*

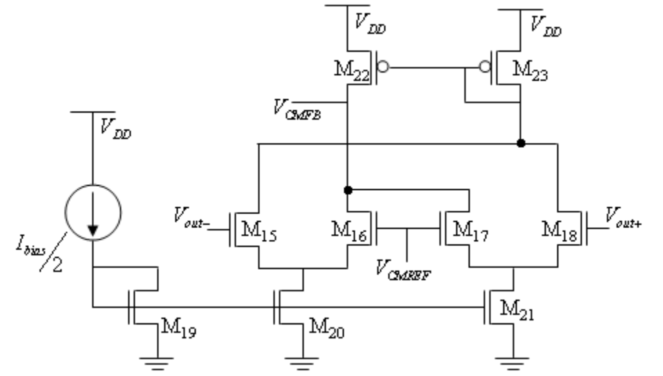

Fig. 6. *Schematic of continuous-time common mode feedback circuit*

III. Simulation Results

The circuit was simulated using Cadence SpectreS simulator with BSIMSOI version 3.1 level 11 transistor model. Since the designed amplifier gain is 40dB or 100, we set C_1 to 5pF and C_2 to 50fF. The lower parasitic capacitances in FD-SOI process enable use of smaller capacitances in design of amplifier, significantly reducing the area of the amplifier. The 9pF capacitors are used as load capacitor, C_L. Figure 7 presents the simulated transfer function of neural amplifier. Table 2 shows the performance summary of the designed neural amplifier. The gain was simulated as 39.5 dB in passband, from 0.000635Hz to 7.1kHz. The simulated phase margin was 78 degree. The low cutoff frequency is 0.000635Hz which is quite low due to very high resistance of symmetrical resistor. Since we use only 2μA as biasing current total supply current is almost 4μA leading to total power consumption of 6μW. The current consumption from biasing circuits are excluded here. Integrated input referred noise was simulated as $3.07\mu V_{rms}$ and the noise efficiency factor(NEF) is calculated as 2.8. $1/f$ noise parameters were not available, but we are expecting that $1/f$ noise contribution would not increase the noise level significantly, as shown in [3]. The layout of the amplifier occupies area of 0.004 mm^2 and is shown in Figure 8.

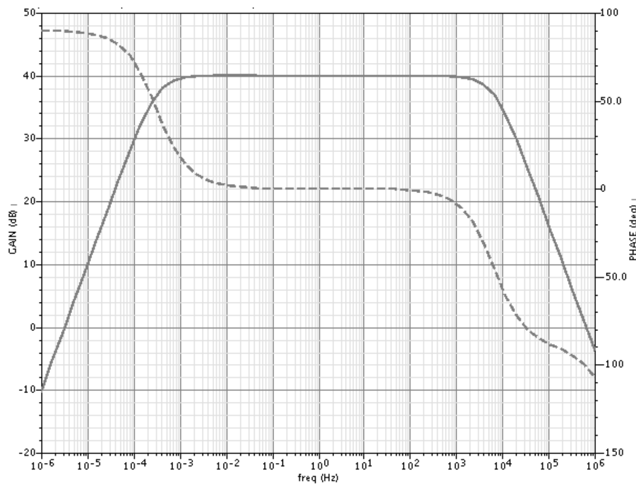

Fig. 7. *Simulated transfer function of amplifier. Midband gain is 39.5dB. Low frequency rolloff occurs at 0.000635Hz, high frequency rolloff at 7.1kHz. Phase margin is 78 degrees.*

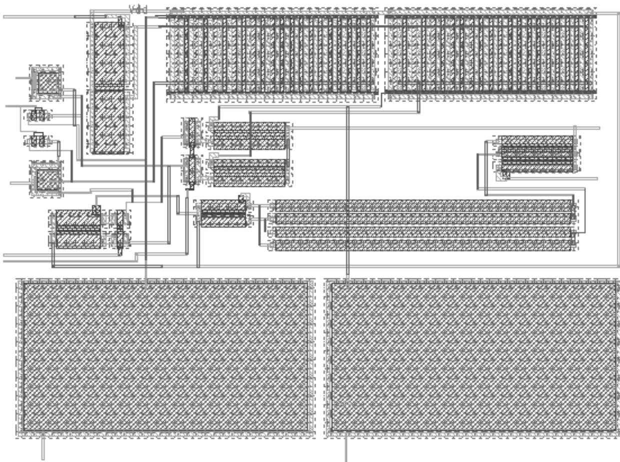

Fig. 8. *Layout of the designed neural amplifier.*

Parameter	Neural Amplifier in SOI
Supply voltage	1.5V
Supply current	4μA
Gain	39.5dB
Phase margin	78 degree
Low frequency cutoff	635μHz
High frequency cutoff	7.1kHz
Input referred noise(μV_{rms})	3.07
Noise efficiency factor	2.8
Area	0.004 mm^2

Table 2: *Performance summary of designed neural amplifier*

IV. Conclusion

Modern implantable neural recording systems should accommodate thousands of recording channels to be able to record signals from large populations of neurons. The neural amplifier, most critical components in the design, should consume less power and area, and also have high noise immunity to digital switching in subsequent analog to digital converter, implemented on the same substrate. FD-SOI technology enables design of neural amplifier with better power and noise performance than in bulk technologies. This was demonstrated through design and simulation of a neural amplifier using symmetrical pseudo resistors in MITLL 0.18 μm FD-SOI process. The design is submitted for fabrication.

Acknowledgment

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References

[1] W. F. Agnew and D. B. McCreery, "Neural Prostheses, Fundamental Studies," New York: Prentice-Hall, 1990.

[2] RP.Wider,EV.Jones,TC.Wind and RF.Edlich, "Functional electrical stimulation cycle ergometer exercise for spinal cord injured patients," Journal of Long Term Effects of Medical Implants, 12(3), pp. 161-74, 2002

[3] R. R. Harrison and C. Charles, "A Low-Power Low-Noise CMOS Amplifier for Neural Recording Applications," IEEE Journal of Solid-State Circuits, Vol.38, No.6, June 2003.

[4] C. Charles and R. R. Harrison, "A Floating Gate Common Mode Feedback Circuit for Low Noise Amplifier," IEEE Southwest Symposium on Mixed Signal Design, pp.180-185, Las Vegas, USA, Feb. 2003.

[5] J. Ji and K. D. Wise, "An implantable CMOS circuit interface for multiplexed microelectrode recording arrays," IEEE J. Solid-State Circuits, vol. 27, pp. 433-443, Mar. 1992.

[6] A. P. Chandran, K. Najafi, and K. D. Wise, "A new DC baseline stabilization scheme for neural recording microprobes," in Proc. 1st Joint EMBS/BMES Conf. Atlanta, GA, Oct. 13-16, 1999.

[7] P. Mohseni and K. Najafi, " A Fully Integrated Neural Recording Amplifier with DC Input Stabilization," IEEE Transactions on Biomedical Engineering, Vol.51, No.5, May 2004.

[8] T.Delbruck and C.A.Mead, "Analog VLSI Adaptive, logarithmic wide dynamic range photoreceptor," in Proceeding of IEEE International Symposium on Circuits and Systems, Vol.4, 1994.

[9] Massachusetts Institute of Technology Lincoln Laboratory, "MITLL low-power FDSOI CMOS process: Design guide," September 2006.

[10] D.Flandre, J.P.Colinge, J.Chen, D.De.Ceuster, J.P.Eggermont, L.Ferreira, B.Gentinne, P.G.A.Jespers and A.Viviani, "Fully-depleted SOI CMOS technology for low-voltage low-power mixed digital/analog/microwave circuits", Analog Integrated Circuits and Signal Processing, vol.21, pp. 213-228, Dec. 1999.

[11] J.P. Colinge, "Fully-Depleted SOI CMOS for Analog Applications," IEEE Transaction on Electron Devices, vol. 45, no. 5, May 1998.