Low-Power High-Resolution 32-channel Neural Recording System

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***Abstract*—A design of low-power 32-channel neural recording system with on-chip high-resolution A/D converters is presented. A neural front-end including low-noise fully differential pre-amplifier, gain stage, and buffer consumes only 56μW. Two 13-bits extended counting A/D converters running at 512KHz sampling rate are integrated with 32 neural front-ends on a chip. The experimental prototype was designed in 0.6μm CMOS process. With a 3.3V power supply, total power consumption of a chip is 22mW and the whole system occupies an area of 3mm $\times$ 3mm.**

I. INTRODUCTION

Recording from large population of neurons using multi-electrodes is indeed becoming a necessary procedure not only to research neuronal activities in central/peripheral nervous system but also to develop neural prosthesis. To better understand how the nervous system functions, we must be able to simultaneously monitor the responses of many neurons in small animals. To utilize advances in fabrication of MEMS structures that enable microelectrode arrays, there is need for recording systems able to record data and communicate gathered information to recording station in such a way that animal movement is restricted in minimal way. VLSI solutions offer low noise, small feature size and modularity. We are investigating design of VLSI microsystem for recording of neural signals from array of microeletrodes mounted on a head of a small animal. The headstage would have data link and would receive power through USB2 cable connection. The chip-on-board technology would be used for volume reduction and would enable interface to different sensor arrays.

The integrated circuits for neural recording have been designed for past decades [1], [2]. There are several design challenges in terms of noise, power, size, and resolution of analog-to-digital converter (ADC) due to the limited design resources. It should accommodate as many processing channels as possible while having properties of low power and low noise. Size and weight were the major constraints in our design. We have designed 32-channel analog neural recording system integrated together with 13-bit extended counting ADC in $3mm \times 3mm$ using 0.6μm CMOS technology.

II. ANALOG SYSTEM DESIGN FOR NEURAL SIGNAL ACQUISITION

Figure 1 represents the schematic diagram of designed 32-channels neuronal recording system. Basically, 16 neural front-ends are multiplexed with one ADC, and the exactly same front-ends and an ADC are duplicated for another 16-channels processing so that total of 32 neural front-ends and two ADCs

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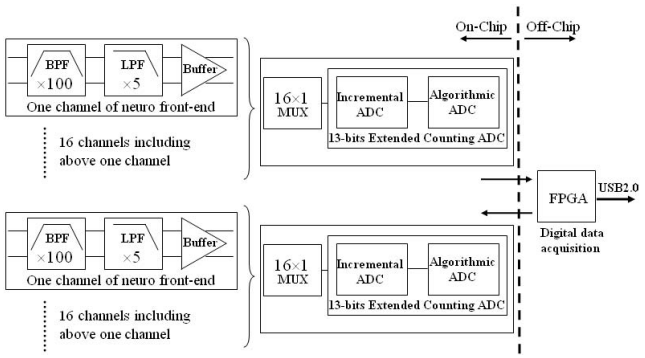

Fig. 1. *Schematic diagram of designed 32 channel neural recording system.*

are integrated on a chip. To communicate digitized neural signals from ADCs, there would be FPGA board interface as well as USB 2.0 connector outside the chip.

Figure 2 shows the schematic diagram for one channel of designed neural front-end. Since the total 32 neural front-ends in the recording system simultaneously process neural signals from 32-electrodes, each channel of neural front-end should consume less power and area, and also have high noise immunity to digital switching in subsequent analog to digital converter on the same substrate. It consists of three parts: (A) pre-amplifier, (B) gain stage and (C) buffer. All three parts use fully differential structures in order to achieve high common mode noise rejection and high noise immunity to digital switching. In the very first stage of the system, pre-amplifier amplifies micro-range (at most 1mV [3], typically 100μV [4]) neural signal from electrode one hundred times and only in the range from 100Hz to 7kHz. This is because extracellular neural action potentials, which we want to record, have frequency components in the range of 100Hz - 7kHz [4], [5]. The gain of this stage is limited by the linearity of pseudo-resistors. Another stage with the gain of 5 is added to maximize the dynamic range before analog-to-digital conversion. The second gain stage also has low-pass frequency characteristic, providing sharper roll-off at cut-off frequency of 7kHz in pre-amplifier. The third part, buffer, is necessary as input stage for ADC.

Figure 4 represents the simulated frequency response for each neuronal recording front-end. It amplifies the neural signal up to almost 54 dB (500 V/V) in the range between 100 Hz and 7 kHz. The second order pole is occurred around 7 kHz so that it rolls off at 40dB/dec.

A. Pre-amplifier Design

Figure 2(A) shows the structure of designed pre-amplifier. It is similar to previous design [6] so that the midband gain A_M is set by C_1/C_2, and the bandwidth by $g_m/A_M C_L$, where g_m

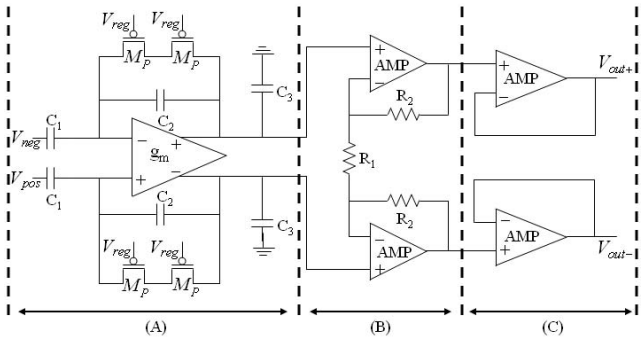

Fig. 2. *Schematic diagram for a channel of neuro front-end including (A)pre-amplifier, (B)gain stage, and (C)buffer.*

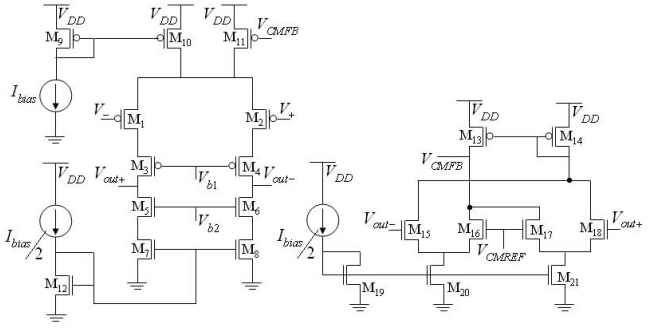

Fig. 3. *Schematic diagram of pre-amplifier with a continuous-time common mode feedback circuit.*

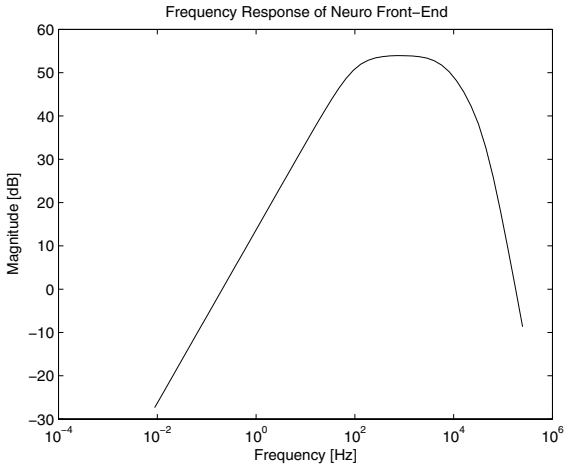

Fig. 4. *Frequency response of a neuro front-end.*

is the transconductance of the operational transconductance amplifier (OTA). To implement very low cut-off frequency high resistive MOS elements (M_P are used. The resistance of PMOS element is up to the order of $10^{13}\Omega$ depending on a biasing voltage (V_{REG}). The total time constant is set to $2R_PC_2$, where R_P refers to resistance of MOS element. Therefore, the low cut-off frequency of neural amplifier is determined by $1/(2\pi 2R_PC_2)$.

For design of OTA in pre-amplifier, fully-differential telescopic operational amplifier, shown in Figure 3, is chosen with consideration of high gain, stability, and low-noise properties. By maximizing the gain of OTA, the effect of parasitic capacitances at the input of OTA could be reduced. It also makes possible to use smaller C1 and C2 capacitors to set a gain. Cascode transistors increase OTA gain without degrading the noise performance. The smaller output voltage swing of the telescopic structure is not critical, since the output voltage swing is limited by the linear range of the high-resistive element (M_P), and not by the telescopic structure. The main trade-offs in this OTA design are between noise, power, and size. If we only consider the power consumption, the maximum performance may be obtained when the value of the transconductance/drain current ratio (g_m/I_d) is the largest. However, the input referred thermal noise of OTA is given as

$$\overline{v_{in,thermal}^2} = \frac{16kT}{3g_{m1}}[1 + \frac{g_{m7}}{g_{m1}}]\Delta f \qquad (1)$$

g_m/I_d ratio and size of transistors should be considered to minimize input referred thermal noise. As total power consumption is determined by biasing current, we have chosen a lower biasing current. From the noise analysis, input transistors M_1 and M_2 should be sized with as large W/L ratio as possible so that a maximum g_m/I_d ratio is obtained. In the same manner, the noise contribution of transistors M_7 and M_8 can be minimized by choosing small W/L ratio or minimizing g_m/I_d ratio. Increasing the length of these M_7 and M_8 transistors is limited by available space. Effect of flicker or $1/f$ noise is minimized by choosing PMOS transistor for inputs and by increasing gate area of the transistors in design.

For the implementation of common-mode feedback circuit, we have chosen continuous-time circuit shown in Figure 3. The common-mode output voltage is set to $V_{DD}/2$ or $1.65V$. If the output common-mode level increases, current of M_{15} and M_{18} will increase and the current of $M_{16,17}$ will decrease. This causes increment in V_{CMFB} and makes the V_{SG} of M_{11} decrease, followed by decrease in common-mode output voltage.

B. Gain stage and buffer design

Figure 2 also shows the gain stage and buffer. The structure of gain stage is basically non-inverting opamp. It has two resistors (R1 and R2) that create gain of 1+(R2/R1). The gain stage also provide additional low-pass filter with cut-off frequency of 7 kHz. There are two stages inside this gain stage: OTA and output pmos source follower to drive resistive loads. The low-pass cut-off frequency is set by both transconductance of the OTA and input capacitance of the source follower.

The gain stage is followed by a buffer which will drive subsequent multiplexer. The gain and phase margin should be considered in this buffer design because the amplified signal should settled down before following ADC starts the data conversion. The folded cascode op-amp is used in this buffer design and it has gain of around 1200 and over 80 degrees of phase margin.

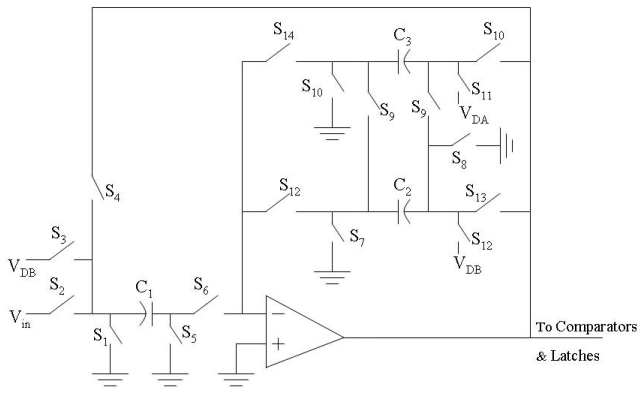

Fig. 5. *Single-ended schematic of ADC.*

III. DESIGN OF LOW-POWER HIGH-RESOLUTION ADC

To reduce the noise introduced in communication, on-chip A/D conversion is required. The neural recording system in this prototype requires a resolution of 13-bit and a bandwidth of up to 1MHz. Area and power are two major constraints in designing the ADC.

Under the specifications stated above, extended counting is chosen as the architecture of our ADC, where a compromise of resolution and speed is achieved [7]. For one A/D conversion, the converter passes through two stages. In the first stage, the converter acts as a first-order incremental converter to convert the most significant bits. Then in the second stage, the same hardware is used to convert the least significant bits by an algorithmic A/D conversion technique.

Figure 5 shows the single-ended schematic of the ADC and figure 6 shows the clock scheme. The implemented fully differential structure is not shown here for simplicity. Compared with the previous reported architecture [7], the number of capacitors is reduced, leading to a smaller size and lower power consumption. All capacitors are nominally equal. C_2 and C_3 are connected together in incremental stage, providing a larger feedback capacitance. 0.5 additional clock cycle is needed, resulting in a total 16.5 clock cycles per A/D conversion.

The power consumption of the ADC is mainly determined by the sampling speed, where the latter one is dictated by the settling time of the OPAMP used within the ADC. In the second conversion stage, two bits are generated in one clock cycle, leading to a settling time of a half of the clock cycle (*T*/2). We assigned one third of the settling time for the slew rate (SR) limited part and the rest of it for the gain bandwidth (GBW) limited part [8]. By using a single pole small signal model, two equations can be derived.

$$I_D = 3 \cdot \frac{1}{T} \cdot V_{pp,diff} \cdot C_{L,eff} \tag{2}$$

$$I_D \cdot \frac{W}{L} = \frac{9ln^2 2}{2\mu_0 C_{ox}} \cdot (\frac{N+1}{T})^2 \cdot (\frac{C_{L,eff}}{f})^2 \tag{3}$$

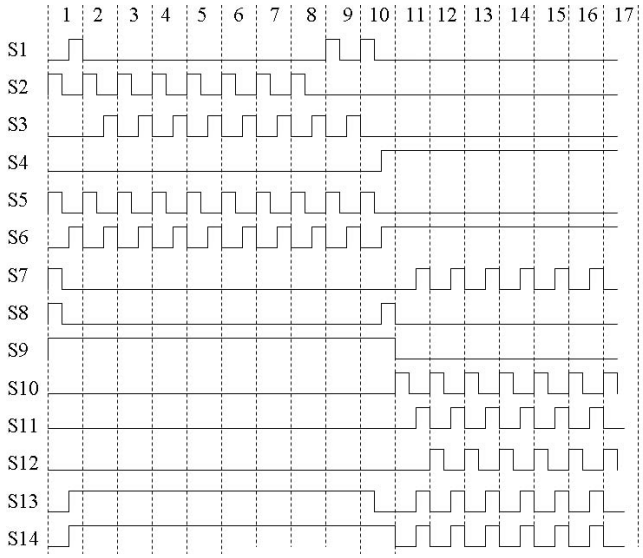

Fig. 6. *Clocking scheme of ADC. The first 8 clock cycles are assigned to incremental stage, while the rest are for algorithmic stage.*

where I_D is the drain current of the OPAMP input differential pair, $V_{pp,diff}$ is the largest differential full scale slewing, $C_{L,eff}$ is the effective load presented at the output of the OPAMP, N is the resolution, and f is the feedback factor. The first equation sets the SR limited current requirement, and the second equation sets the GBW limited current requirement. It can be seen that the drain current is in linear relationship with $(1/T)$ when SR limitation is dominant, and has a proportionality of $(1/T)^2$ when GBW limitation is dominant. Since the number of the ADCs is proportional to the settling time (T), an optimized point can be found. Based on the design process parameters and the unit capacitance used in our design, we determined the optimal number of ADCs through MATLAB simulations.

Figure 7 shows two different circuits used to calculate the effective load capacitance for incremental stage and algorithmic stage, respectively. The capacitors C_S, C_{F2} and C_L are nominally equal, and C_{F1} is two times of C_S. The effective load capacitance of the two stages is equal to [8]:

$$C_{load,incremental} = C_{out} + \frac{C_{F1} \cdot (C_S + C_{in})}{C_{F1} + C_S + C_{in}} \tag{4}$$

$$C_{load,algorithmic} = C_L + C_{out} + \frac{C_{F2} \cdot (C_S + C_{in})}{C_{F2} + C_S + C_{in}} \tag{5}$$

It is clear that the effective load capacitance of incremental stage is lower than that of algorithmic stage. Longer clock period can be assigned to algorithmic stage while maintaining the same OPAMP. If different clock period is not available, two different OPAMPs can be implemented with larger biasing current assigned to the OPAMP used in algorithmic stage.

IV. SIMULATION RESULTS AND LAYOUT

The circuit was simulated using Cadence SpectreS simulator and BSIM3 version 3.1 transistor models are used with $1/f$

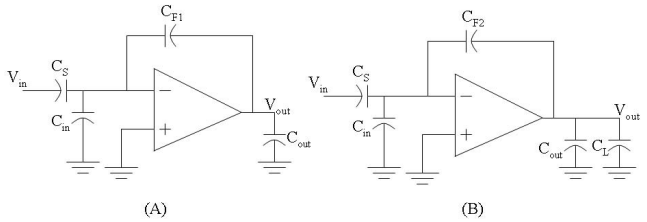

Fig. 7. *Effective load capacitance (A)incremental stage; (B)algorithmic stage.*

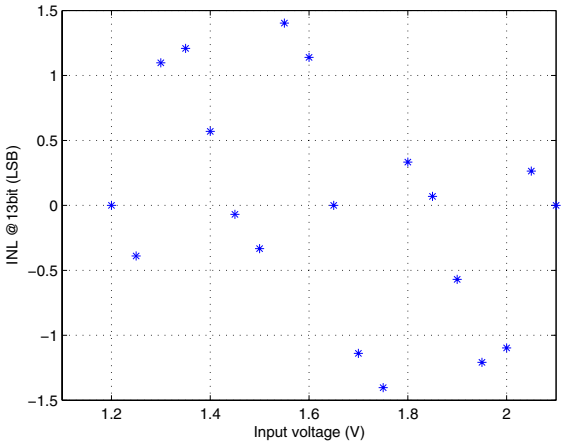

Fig. 8. *Integral nonlinearity(INL) of ADC.*

TABLE II
SUMMARY OF ADC.

Resolution	13 bit
Supply Voltage	3.3V
Clock Frequency	8.4MHz
Sample-frequency	512KHz
Power Consumption	10mW
Input Range	1V
Core area	$0.7mm$ by $0.8mm$

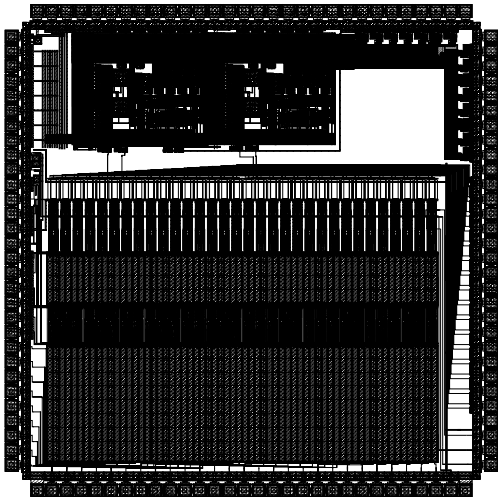

Fig. 9. *Layout of the designed 32-channel neural recording system.*

noise parameter of KF = 6×10^{27} (PMOS), KF = 3×10^{25} (NMOS), and AF = 1 (PMOS and NMOS). TableI summaries the performance of simulated pre-amplifier. Both gain stage and buffer in one channel of neuro front-end occupies only $0.0172mm^2$ and they consume 42.34μW. Total power consumption for single channel of neuro front-end is about 56μW.

Figure 8 shows the simulated integral nonlinearity(INL) of ADC. The x-axis is the input voltage, swept from 1.2V to 2.1V, with a step size of 50 mV. The Y-axis is the corresponding INL in unit of 1 LSB at 13 bit. TableII presents the performance summary of the designed ADC. Figure 9 shows the whole system layout submitted for fabrication.

V. CONCLUSIONS

This work presents a design of low-power neural recording system mounted as head-stage on small animal, with on-chip 13-bits extended counting A/D converters. All 32 channels of neuro front-ends and two 13-bit A/D converters are successfully integrated into a $3mm$ by $3mm$ chip area in 0.6μm CMOS process.

TABLE I
PARAMETERS FOR SIMULATED PREAMPLIFIER.

Parameters	Perfomances
Gain	39.5dB
Gain bandwidth	$100Hz$ to $7kHz$
Input noise	$3.35\mu V_{rms}$
Power consumption	13.68μW
Noise efficiency factor	3.18
Phase margin	105 degree
Area	$0.0482mm^2$

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