16-CHANNEL WIDE-RANGE VLSI POTENTIOSTAT ARRAY

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ABSTRACT

A 16-Channel current-measuring VLSI sensor array system for electrochemical detection of electroactive neurotransmiters like dopamine and nitric-oxide is presented. The designed ADC architecture is first-order single bit delta-sigma modulator with programmable oversampling ratio. The modulation of feedback duty-cycle in modulator design enables choice of current range in accordance to magnitude and time constant of signal leading to current range that spans over six orders of magnitude and sensitivity up to picoamperes at hundred millisecond conversion time with power consumption of 300 μW. A 3mm x 3mm chip in 0.5 μm CMOS technology is used for real-time multi-channel acquisition of neurotransmitter concentration.

1. INTRODUCTION

Transmission of signals in neural pathways is mostly electrical in nature with the exception of synapses, the non-conductive gaps between adjacent neurons. Neurotransmitters are a class of biomolecules that carry signals across the synaptic gap between neurons in the nervous systems of all living organisms. Studies of neural pathways and the etiology of neurological diseases, like epilepsy and stroke, require real-time and sensitive detection and monitoring of neurotransmitters. Several methods like fluorescence imaging, immunochemical, liquid chromatography are used to detect and measure neurotransmitter activity. Certain electroactive neurotransmitters (eg Nitric Oxide, dopamine) are amenable to detection via electrochemical analysis. Electrochemical analysis of neurotransmitters is very attractive due to high sensitivity, rapidity and the ability to perform distributed measurements [1, 2, 3].

Electrochemical analysis is based on the fact that in solution certain species can undergo a chemical reaction on the surface of an electrode held at a characteristic potential. This characteristic potential depends on the species and is called the oxidation or reduction potential depending on whether the reaction involved a gain of electrons (oxidation) or a loss of electrons (reduction). In general this is the *redox potential*. The electron transfer causes a *redox current*, proportional to the concentration of the species, to flow through the electrode towards or from the source maintaining the redox potential. The currents range from picoamperes to microamperes and have a slow time scale ranging from milliseconds to seconds.

Electroanalysis involves a potentiostat that can measure the redox current while maintaining the redox potential. Currently electrochemical analysis of neurotransmitters is done using a large benchtop potentiostat. Analysis is limited by the size, sensitivity and cost of the instruments. The ability to record neurotransmitter levels from a population of neurons, rather than a single cell, is of tremendous potential. Sensor arrays can be microfabricated to perform high spatial resolution sensing. Accordingly multichannel potentiostats are needed to be able to process the signals from the sensor arrays. VLSI offers high sensitivity, small feature size, low noise, low power and modularity. Integrated potentiostats with one or few parallel channels have been previously reported by others [4, 5] and our group [6, 7].

2. CHIP ARCHITECTURE

The currents of interest range from picoamperes to microamperes, with time scales ranging from milliseconds to seconds. The current span of several orders of magnitude calls for different scales of measurements and the long time constants enable long integration times.

A block diagram of one channel of potentiostat array is shown in Figure 1. The AD converter implemented is current-measuring first-order single bit delta-sigma modulator. The choice of the modulator is driven by low-frequency content of the signal of interest, which allows high oversampling ratios and trade-off between bandwidth and resolution. The high-frequency noise is reduced in digital domain together with shaped quantization noise. Single-bit quantization leads to very robust circuits, less sensitive to matching and imperfection errors. The first-order modulator is also amenable to simple and compact implementation. The sampled-data switched-capacitor (SC) realization offers low-noise and low-power implementation.

To achieve wide dynamic range of currents with multiple scales, as alternative to using imprecise current mirrors, we have chosen to insert a time-modulation in the feedback loop, a variable time-period over which the feedback is active. This introduces a programmable gain of input current with respect to reference current of DA converter, as a small input current is to be integrated over longer time period, while a reference current is integrated over

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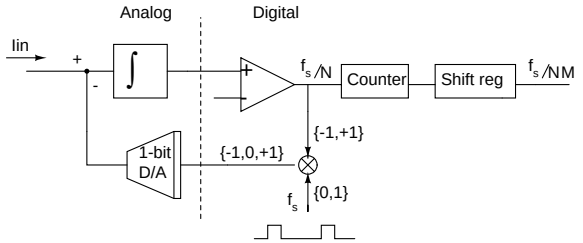

Fig. 1. Implementation level diagram of a single channel of the potentiostat.

shorter time interval. Using programmable duty-cycle for the same reference current and clock frequency, the chip is capable of handling wide range of currents.

The decimator is implemented using binary counter and the digital value is stored in a register at the end of the conversion cycle. The choice of a binary counter as decimator eliminates the problem of spurious tones possible with steady inputs. The value is read from the buffer in serial fashion asynchronously from all 16 channels using shift register.

2.1. Delta-sigma modulator

The first-order delta-sigma modulator consist of current integrator, comparator and switched-current 1-bit DA converter. The integrator design with switched-current DAC, controlled by clock with programmable duty-cycle, is shown in Figure 2. The measured current is integrated on capacitor C_1. The capacitor C_2 provides a high input conductance virtual ground node at reference voltage V_{ref} and samples the input offset of the amplifier. The dominating noise source, 1/f noise, is reduced by correlated-double sampling (CDS) technique. 1-bit DA converter is implemented using switched current sources, transistors M_1 and M_2. The current sources are always turned on, decreasing the effect of charge injection noise. Transistors M_3, M_4, M_5 and M_6 are minimum size switches that direct the reference current into integrator or reference voltage source. Biasing voltages V_p and V_n are set with the single externally supplied current reference.

In the reset phase, at the beginning of the conversion cycle, clock $intClk_1$ is low. The input node is precharged to reference voltage V_{ref} and integrating capacitor C_1 is precharged to mid point of the voltage range, zero voltage level V_{mid}. In the conversion phase, when clock $intClk_1$ is high, capacitor C_2 provides a virtual ground at the input node and input and reference current are been integrated on capacitor C_1. In the conventional delta-sigma design, the reference current of DA converter is integrated for the whole period of oversampling clock in the direction determined by the output bit D, obtained by comparison of the integration voltage V_{int} and zero voltage level V_{mid} at the rising edge of oversampling clock. The maximum input current to be measured in this case is equal to reference current. For different range of the currents to be measured, the reference current has to be changed accordingly. Instead of integrating the reference current

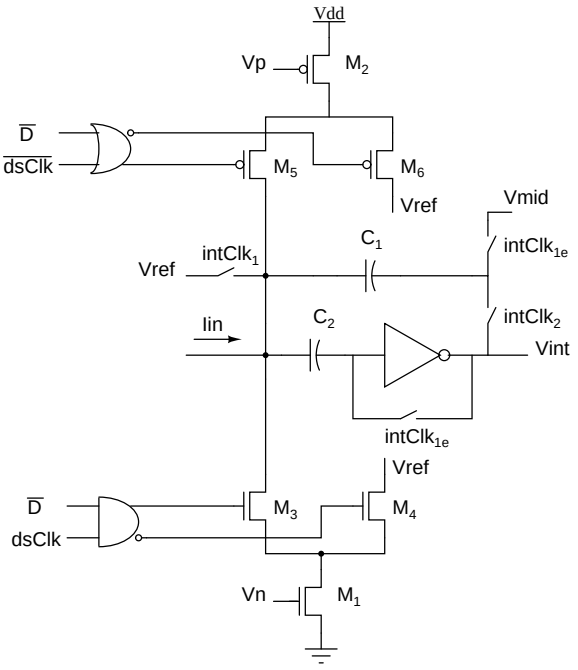

Fig. 2. The schematic of sigma-delta current integrator with programmable gain control.

over the whole period of oversampling clock, we propose to integrate it over time that is ratio of this period. This has the same effect on the integrated voltage as the change of the reference current of 1-bit DAC. Effectively, we introduce a gain of input current, integrated through the whole period of oversampling clock, with respect to reference current. In proposed implementation, the 1-bit results of comparison between integrated voltage and zero voltage level are multiplied with the oversampling clock, which becomes a feedback control clock that activates the feedback loop only when it is high. The reference current is now being integrated only when oversampling clock $dsClk$ is high and by varying the duty-cycle of this clock we vary the gain of the input current, enabling multiple scales with the same reference current. Clock $dsClk$ is derived from the system clock of frequency f_s and it is high for one period of the system clock. The oversampling clock is low for time equal to N multiples of a period of the system clock. N represents the digital gain of the input current with respect to reference current of DA converter. In the Figure 3, we illustrate the feedback-control clock, time-modulated feedback signal and output voltage of the integrator for two different values of digital gain N. By adjusting the programmable duty-cycle for the same reference current and system clock frequency, the chip is capable of handling wide range of currents. The gain N can be set anywhere between 1 and 65536.

Conversion clock $intClk$ is derived from oversampling clock $dsClk$ and their ratio defines the oversampling ratio. The oversampling ratio can also be set anywhere between 1 and 65536. The clocks $intClk_1$ and $intClk_2$ in Figure 2 are non-overlapping clocks derived from the clock $intClk$. The clock $intClk_{1e}$ is

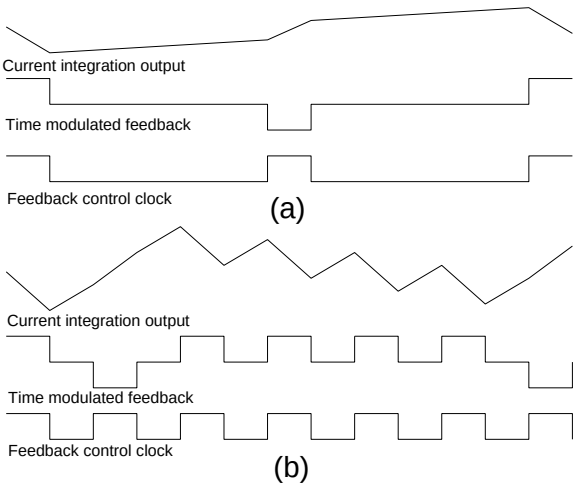

Fig. 3. Time-modulation of the feedback signal for two different values of digital gain N.

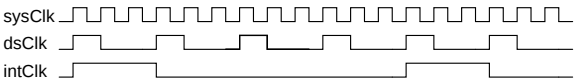

Fig. 4. The programmable duty-cycle clock $dsClk$ and integration clock $intClk$. The gain is 3 and oversampling ratio is 4 in the depicted case.

the replica of clock $intClk_1$ with its rising edge following the rising edge of $intClk_1$ and its falling edge preceding the falling edge of the clock $intClk_1$. The clocks are illustrated in Figure 4 for the value of the gain of 3 and for oversampling ratio of 4.

The high gain amplifier is single-stage cascoded inverter operating in the subthreshold region. It offers low-noise and low-power solution, as well as high density of integration. The gain of the inverter is sufficient for specified resolution.

The voltage reference V_{ref} that sets the voltage level of the virtual-ground current input is jointly set for 4 channels. Gain and oversampling ratio are same for all 16 channels.

The comparator design is shown in Figure 5. The comparator is reseted at the beginning of each integration cycle to zero level voltage V_{mid}. The result of comparison between integrated voltage and voltage V_{mid} is latched at the end of period of clock $dsClk$. The high-gain amplifier used in comparator is also a single-stage cascoded inverter.

2.2. Decimator and Serial Output

The decimator is implemented as the simple accumulate-and-dump circuit. The output bits of delta-sigma modulator that represent logic one are counted using 16-bit counter during one conversion period. The conversion period is programmable and represents the period of clock $intClk$. At the end of each conversion cycle, the counter value is written to output register and a new conversion cycle begins with cleared counter. The register can be read asynchronously at any time during conversion cycle.

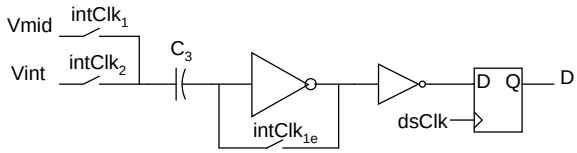

Fig. 5. Schematic of delta-sigma comparator.

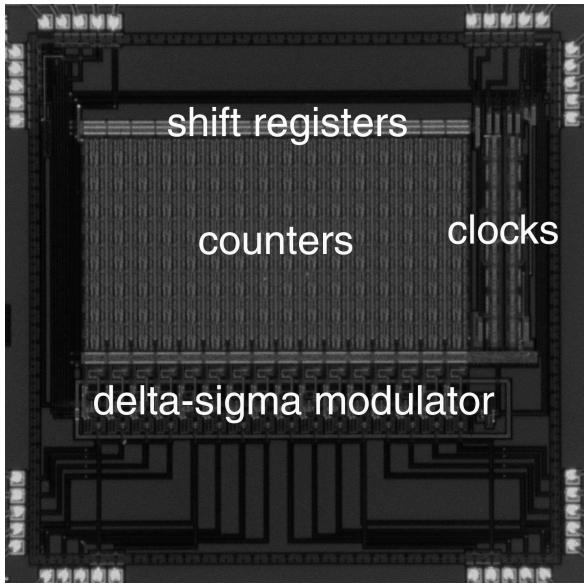

Fig. 6. Micrograph of 3×3 mm^2 chip in 0.5 μm CMOS technology.

The 16 bits representing the digital value of input current of each channel are shifted out bit-serially using clock independent of system clock and 256 cycles are necessary to read out all 16 channels.

3. EXPERIMENTAL RESULTS

The 16-Channel VLSI potentiostat measures 3×3 mm^2 in 0.5 μm CMOS technology. Figure 6 depicts the micrograph and system floorplan of the chip.

To demonstrate precision and wide dynamic range of currents over few scales using programmable feedback duty-cycle period, the input current was swept from picoampers to microampers. In Figure 7 we show the normalized digital output of the chip as function of input current, for wide range of gains and resolutions. The input current was swept in logarithmical fashion using Keithley SourceMeter model 6430 (Keithley Instruments Inc., Cleveland, OH). The gain, OSR, the range of input currents that can be handled by those parameters and conversion time are shown in Table 1 for each of the traces. The reference current was set to 0.6 μA and the system clock frequency f_s was 2 MHz. The input potential V_{ref} was set to 1 V.

The chip was used for potentiostatic measurements of the neurotransmitter Dopamine in a phosphate buffered solution (PBS). A standardized solution of Dopamine with concentration 1.055mM and a standard Ag/AgCl reference electrode were used. The preparations are described elsewhere [7]. Commercially avail-

Trace	*Gain* (G)	*OSR*	*Input current range*	*Conversion time* (ms)
A	2^0	2^{16}	$\pm$500nA	32
B	2^2	2^{15}	$\pm$125nA	65
C	2^4	2^{14}	$\pm$30nA	131
D	2^6	2^{13}	$\pm$8nA	262
E	2^8	2^{12}	$\pm$2nA	524
F	2^{10}	2^{11}	$\pm$500pA	1048
G	2^{12}	2^{10}	$\pm$125pA	2097
H	2^{14}	2^9	$\pm$30pA	4194
I	2^{16}	2^8	$\pm$8pA	8388

Table 1. Parameters for characterization traces shown in Fig. 7.

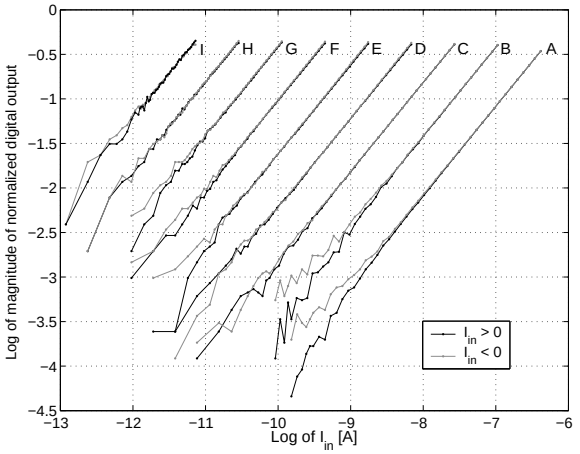

Fig. 7. Normalized digital output of the chip for several values of gain, OSR and input currents.

able carbon microfiber electrode (CF 30-250, WPI Inc, Sarasota, FL) was used as the sensor. The sensor and the reference electrode were immersed in the PBS solution and boluses of the dopamine solution were added (shown by the arrow marks on Fig. 8) into the PBS at fixed intervals.

4. CONCLUSION

We presented a 16-Channel potentiostat array with a wide dynamic range of currents that span through six orders of magnitude and sensitivity of 1 pA. The current range is digitally controlled through programmable feedback duty-ratio cycle. The potentiostat chip can be used to acquire real-time multichannel data from microfabricated neurotransmitter sensor arrays.

5. ACKNOWLEDGMENTS

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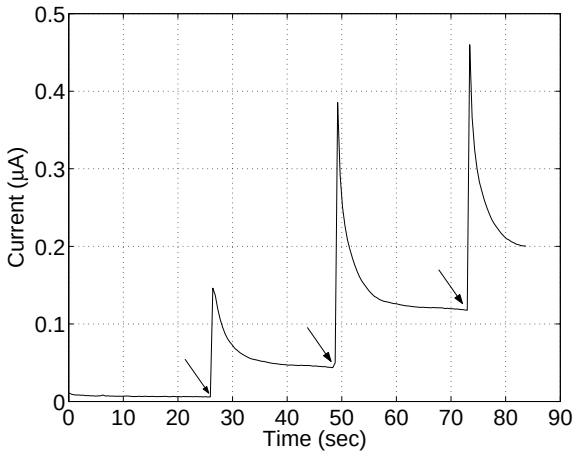

Fig. 8. Real time neurotransmitter monitoring by the chip using the commercial CF 30-250 as the working electrode. The arrow marks denote times of 1μL dopamine addition.

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