

JUAN CARLOS OCHOA

86 Smith Ave, Bay Shore, NY 11706

Available to relocate

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Objective

To obtain a position as an Electrical Engineer.

Computer Skills

- **Programming Languages:** Verilog, VHDL, PERL, C, C-shell, awk, sed, DOS batch, and html.
- **Operating Systems:** Solaris, Sun, VAX/VMS, X-Windows. Windows NT Workstation/Server, 9x, 00, and XP.
- **Engineering Software:** Synopsys Library Compiler, Design Compiler, Design for Test (DFT) Compiler, TetraMAX, Power Compiler, Formality, and Test Compiler. HSPICE, SiliconSmart CellRater (CR), MATLAB, Cadence Verilog-XL, Sequence Design PowerTheater Analyst, Debussy, WorkVIEW's VHDL SpeedWAVE, Maple, LabVIEW, and Acolade.
- **Commercial Software:** Microsoft Office, MKS Toolkit, Hummingbird Exceed and NFS Maestro Client, PowerQuest Drive Image Pro, Norton Ghost, Corel Draw, Adobe PhotoShop, and Lotus Notes.
- **Network Protocols:** TCP/IP and DHCP.

Work Experience

- Standard Microsystems Corporation, NY

Jul 97-Jan 04

Design Automation Engineer.

- Supported all phases of DFT and Automated Test Pattern Generation (ATPG). Validated TetraMAX's Verilog testbenches and conversions from STIL testbenches to LTX tester patterns.
Major accomplishments: Integrated insertion and testing of scan chain circuitry into company's methodology. Test vectors generated tested successfully at least a dozen chip designs.
Relevant training: Synopsys Design Compiler, DFT with DFT Compiler, ATPG with TetraMAX, and Test Compiler.
- Developed a tool to characterize and model standard cells for timing, constraints, and power. Programmed in Perl and C-shell. Characterized via HSPICE CMOS standard cells in technologies from 0.5 to 0.18 microns. Modeled standard cells in Synopsys Library Compiler and Verilog.
Relevant training: SiliconSmart CR. Advanced PSPICE. Verilog Language and Synthesis. Synopsys Library Development, Chip Synthesis, Power Compiler, and Formality. Sequence Design PowerTheater Analyst. Esperan's Low Power Design.
- Supported a translator from test vectors to ATE patterns. Programmed in C and Makefile.
Major accomplishments: Ported translator from Solaris to Sun OS and VAX/VMS. Integrated virtual signals, user-defined logic combinations of signals, and mapping of output states to non-traditional logic states. Fixed and enhanced precision by allowing sub-nanosecond timings. Developed an LTX tester output formatter. Updated translator's input readers: Cadat BSO, Genrad, Sentry, SOM, Tabular Data, and WorkVIEW's ViewSIM. Repaired translator's output formatters: Advantest, Cadat, Genrad, Sentry, SOM, and Trillium.
- Developed a GUI based MATLAB Statistical Characterization Toolbox.
- Qualified software releases and tools before introducing them into IC design flows.
- Administered Design Engineering's Windows PC network. Built and upgraded all PCs. Supported all network users with PC hardware and software issues. Managed network security and interconnectivity with a Solaris network. Advised superiors on software and PC hardware purchasing and productivity enhancements.
Major accomplishment: reduced PC build time from a couple of work-days to a couple of hours.

JUAN CARLOS OCHOA

- State University of New York at Stony Brook, NY Jan 97–May 97
Computer Architecture Teaching Assistant (TA). Taught ASIC design via VHDL.
Analog and Digital Control System Design TA. Taught analysis and design of control systems.
- Polytechnic University, NY Aug 95–Jun 97
Computer Lab TA. Supported UNIX and Windows computer users.
Engineering Lab TA. Taught LabVIEW virtual instruments development.

E d u c a t i o n

- Polytechnic University (formerly "Brooklyn Poly"), NY
Master of Science in Computer Engineering. GPA 3.5. Jan 98–Dec 01
- State University of New York at Stony Brook, NY
Master of Science in Electrical Engineering. GPA 3.47. Aug 96–Dec 97
- Polytechnic University, NY
Bachelor of Science in Electrical Engineering. GPA 3.46. Aug 93–Jun 96
- Suffolk County Community College, NY
Associate of Science in Electrical Engineering. GPA 3.8. Aug 91–Jun 93
Applied Associate of Science in Electrical Technology. GPA 3.7. Feb 88–Jun 91
- San Carlos University, Guatemala, Central America
63 credits in Mechanical–Industrial Engineering. Jan 84–Nov 86

P e r s o n a l

U. S. citizen. Fluent in Spanish and Portuguese.

References will be furnished upon request.