Introduction and Comparison of CCD and CMOS

Image Sensors

Written report of ECE558 by Ning Gu (104693975)

Submitted to Prof. Murali Subbarao
Abstract: This report provides an introduction of the working principle of both CCD and CMOS imager which are widely used in image acquisition. The performance and the cost of both devices and the according systems are compared.

1 Introduction
CCD (Charge Coupled Device) and CMOS (Complementary Metal Oxide Semiconductor) image sensors are two different technologies for capturing images digitally. While they are often seen as rivals, CCDs and CMOS imagers have unique strengths and weaknesses that make them appropriate to different applications. Neither is categorically superior to the other, although vendors selling only one technology often claim otherwise. The choice depends far more on the application...and the vendor.

Both types of imagers convert light into electric charge and process it into electronic signals. In a CCD sensor, every pixel's charge is transferred through a very limited number (often one) of output nodes to be converted to voltage, buffered, and sent off-chip as an analog signal. All of the pixel can be devoted to light capture, and the output's uniformity (a key factor in image quality) is high. In a CMOS sensor, each pixel has its own charge-to-voltage conversion, and the sensor often also includes digitization circuits, so that the chip outputs digital bits. These other functions reduce the area available for light capture, and with each pixel doing its own conversion, uniformity is lower. But the chip requires less off-chip circuitry for basic operation.

2 CCD Technologies
Since the early 1970's, Solid State imaging systems have primarily been utilizing Charge Couple Device (CCD) technology for the imaging component. CCDs use the inherent photoresponsiveness of silicon to convert incident photons into electrons. Implants in the silicon and voltage biases on polysilicon gates confine the generated electrons to discrete packets. These gates are then sequentially clocked and the individual packets of charge in each pixel eventually travel to an output amplifier. In an imaging 2-D array this is usually accomplished by keeping columns separate by an implant and transferring each row of data into a serial multiplexer. Once the serial multiplexer transfers a line of data to the output amplifier the next row is transferred into
the serial multiplexer. The output amplifier proportionally converts the electrons into an output voltage. A CCD is an analog device. The clocks required to clock the gates often have rail voltages of various levels such as +4, -8, -12, etc. and the output amplifier has its own set of “non-standard” DC bias levels. This architecture helps explain some of the advantages and disadvantages of CCDs as imaging devices. Because each charge packet is separated by implants and gate voltages, an excess amount of charge can spill over to adjacent potential wells. This effect is seen as blooming and takes place in the column direction. Also, the transfer of charge is not perfect. A small amount is left behind during every transfer.

On large arrays at high clock speeds this becomes noticeable and can show up as a smearing of the image. Since every charge packet is transferred to the same output amplifier the global uniformity of the image is very good, meaning the fixed pattern noise is quite low. It also means that this one amplifier must have all of the device gain and a very high bandwidth, allowing for a high white noise because every pixel in the array must be amplified within a single frame time.

Technology advances with CCDs (Charge Coupled Device), like increased resolution at lower manufacturing costs, have fueled the growth in the electronic imaging industry. However, some of the typical constraints of CCDs remain unchanged, such as the very low output signal level and the inherent noise sources. Furthermore, increased resolution generally equals higher read-out speed, which intern dictates the requirements for the subsequent electronics.

The CCD is the central element in an imaging system. Designers need to be aware of the special requirements for the signal conditioning of the CCD in order to achieve the maximum performance. The output signal of the CCD is a constant stream of the individual pixel “charges” and this results in the typical form of stepped DC voltage levels. This output signal also contains a DC-bias voltage, which is in the order of several volts. The signal is then passed through a capacitor to block the DC voltage before going into the preamplifier. To maintain the necessary relationship between the pixel information and the baseline, a clamp or DC-restore circuit is usually situated in the first processing stage. The next stage is used as a noise reduction circuit specific to CCD based systems: the correlated double sampler (CDS). Following is another gain stage, which could be a
automatic gain control amplifier (AGC), or a fixed gain stage with offset adjustment. Before going into the A/D converter it usually passes through a dedicated buffer or driver circuit optimized for the selected converter type. Further baseline stabilization can be achieved by having a D/A converter in a digital control loop. In the following discussion the CCD itself is looked at and design techniques are explored.

In its principle, the operation of a CCD array is quiet simple. A common analogy is shown here, using an array of buckets on conveyor belts. During a rain shower the raindrops will fill the lined up buckets more or less. Then the conveyor belts transport the buckets to the front belt and dump their content into another row of buckets. As they move forward the rainwater is spilled into the metering glass. The scale on the metering glass indicates how much water was collected in the individual bucket. When relating this model to a real CCD element, the “raindrops” are the light (photons) falling onto the CCD surface, the buckets are the many pixels of a CCD array and the “conveyor belts” are the shift registers that transport the pixel charge to the output stage. This output stage is mainly the sense capacitor, here the “metering glass”, and an output source follower is used to buffer this sense capacitor.
The CCD array is configured into multiple vertical shift registers and usually one horizontal shift register, both requiring different clock patterns. The flow is as follows: the pixel converts the light (incoming photons) into electrons which are stored as electrical charge. Then the charge is transferred down the vertical register in a conveyor-belt fashion to the horizontal shift register. This register collects one line at a time and transports the pixel charges in a serial manner to the on-chip output stage. The on-chip output converts the charge into a voltage. This voltage is then available at the output in the typical CCD pulse form.

With the standard CCD, most of the pixels can detect the light. The CCD also has small sections at the beginning and at the end of each vertical segment that are covered and therefore “optically black”. Those pixels will always have the voltage level representing black. Some image circuits use those as reference pixels to adjust the signal offset.

Some numbers:

The horizontal read-out speed for systems with up to 12-bit resolution is up to 10MHz. For higher resolutions (£16-bit) the clock speed is around 1MHz.

Typical pixel dimensions are: ~27mm2 for a 512x512 array or ~12mm2 for a 1024x1024 array.
Shown here is the conceptual schematic of the output stage inside the CCD element. This stage is responsible for the so called ‘charge detection’. As discussed earlier, the charge e→ generated is moved into the horizontal shift register. The charge of each individual pixel is controlled by the horizontal clock and stored onto the Sense Capacitor (CS). A typical value for such a capacitor is 0.1pF to 0.5pF. According to $V = Q/C$, the charge will develop a voltage across capacitor CS, representing the light intensity for the particular pixel. A MOSFET transistor configured as a source follower buffers the capacitor from the output node, which connects to the load resistor, RLOAD. At this point, the image (video) signal becomes available at VOUT for further signal processing.

As indicated in the figure above, the output voltage is a series of stepped DC voltages. One pixel period is composed of three different levels: (1) the “reset feedthrough”, (2) the “reference level”, (3) and the “pixel level”.

A readout sequence begins with the reset. Where the FET-switch is closed, set the sense capacitor to the initial reference voltage. The reference voltage can be relatively high, up to +12V. The closing of the switch causes the reset feedthrough, a result of capacitive coupling through the MOSFET. After the decay of this feedthrough the capacitor will reflect the reference voltage level (2). Once the capacitor has been reset, the switch opens and pixel charge is transferred to the capacitor, altering its voltage.

An important specification for CCD elements is the sensitivity. This is a measure of the
achievable output voltage per electron, \( SV = \frac{V_{OUT}}{e} \). With a 0.1pF capacitor, the output voltage would be \(-1.6?\) V per electron. Unfortunately, the source follower has a gain of less than 1 (~0.8).

![Basic CCD Theory](image)

Fig. 4 Build in CCD output stage

The lower limit of the dynamic range in an image system is set by the noise floor. Different techniques are available to maximize the dynamic range and optimize for the input range of the A/D converter, but a thorough understanding about the noise sources is crucial. The main noise source, besides digital feedthrough, is the so-called kT/C-noise of the FET reset switch caused by its channel resistance.

The MOSFET also contributes noise — the flicker (1/f) noise and some white (thermal) noise. Additionally, each resistor is a source of thermal/white noise. Another limit is set by the quantization noise of the A/D converter. The rms quantization noise is expressed by the equation \( q/\sqrt{12} \), with \( q \) being the bit size or LSB weight of the converter. For example, a 10-bit converter with a fullscale input range of 2V has a bit size of \( 2.0V/1024 = 1.953mV \). Hence, the quantization noise is \( 564mV \) rms. Assuming a 0.1pF sense capacitor the detection limit would be at about 350 electrons due to the quantization noise.

One obvious way to reduce this limitation is to use an A/D converter with a higher resolution, e.g., 12 bits.

Another example for a noise source would be the line frequency with 50Hz or 60Hz.
Looking again at the built-in output stage of the CCD, we can identify the different noise sources previously discussed.

- **RESET NOISE**: The thermal noise of the channel resistance (RON) of the FET switch (SW). This noise is often termed as kT/C-noise. With a typical value of 100 to 300 electrons (rms), this is the dominant limitation for the detection of small signals.

- **FLICKER NOISE**: Also 1/f-noise. Originates in the MOSFET, and relates to the presence of traps associated with contamination and crystal defects in the semiconductor. Its magnitude is therefore process dependent.

- **WHITE NOISE** also known as resistor noise: It is temperature dependent and equal to $\sqrt{4kTRB}$. White Noise has several origins. For example, the noise of the load resistor (RL).
3 CMOS Technologies

The proliferation of the next generation of imaging systems has been greatly accelerated by the implementation of Complimentary Metal Oxide Semiconductor (CMOS) imagers. These devices are fabricated right alongside chips for modems, fax engines, cellular phones and microprocessors. And, with these economies of scale come subsequent cost reductions. Ever since imager chip designs have improved and design rules have shrunk to sub-micron levels resulting in increased functionality within the pixel site, the image quality of CMOS imagers can now compete with CCDs. CMOS imagers are, practically, more of an imaging system rather than just a sensor. A CMOS imager typically consists of an imaging core (similar to a CCD in that discrete signal levels are multiplexed to a single output), all of the timing logic, usually requiring only a single clock for operation, on-chip programmability of features such as gain, integration time, and windowing, and an Analog to Digital Converter. Indeed, when a designer purchases a CMOS imager, its not like buying an ECL NAND gate or a TTL SRAM, but an entire system consisting of an imaging array, logic registers, memory, timing generators, and an ADC. Imaging system integration on a chip not only has the advantage of lower power dissipation but also a smaller BOM, less required space, and overall lower cost compared to a conventional CCD imaging system.

CMOS imagers have an amplifier within each pixel site. This converts the discrete charge
packets into a voltage at a much lower bandwidth, needing to reset only at the frame rate. Because of this lower bandwidth the signal to noise ratio is increased which is an advantage of CMOS imagers. Early CMOS imagers, due to larger process geometries than today, did not have this amplifier within the pixel site. This technology, known as Passive Pixel Sensor (PPS), had poor noise performance and was responsible for the early criticism of CMOS imagers.

But today, with the decreased process geometries, increased pixel complexity is possible. Additional features can be added within the pixel site including electronic shutter, Trans-impedance amplifiers, and sample-and-hold circuitry to decrease fixed pattern noise. Indeed, at CONEXANT, on an advanced CMOS imager design with six transistors per pixel, read noise levels of one electron have been measured. The increased amount of circuitry within the pixel has reduced the area available for the light sensitive diode. The decrease in this ratio (a.k.a. fill factor) has been obviated by the use of micro-lenses; tiny lenses fabricated on each pixel site which re-directs the incident illumination that would have otherwise fallen on interconnects or transistors back to the photo sensitive diode area.

An additional advantage of CMOS imagers is the inherent anti-blooming since the charge is contained within the pixel site. The voltage that is generated within the pixel site is switched first onto a column buffer and then to the output amplifier. Since the voltage is switched directly to the output amplifier there is no loss of charge during transfer and
subsequently no image smearing. The drawback is that each amplifier in every pixel has slight differences in threshold voltage creating offsets that result in fixed pattern noise. As designs and processes improve this effect has dramatically been reduced.

Fig. 8. Noise level to be competitive with CCDs.

Due to this functional integration, many imaging applications are now feasible that would not have been practical in times past. Children’s toys, more discrete security cameras, cameras embedded in monitors and laptop computer displays, cellular telephone cameras, fingerprint recognition systems, and even disposable cameras in medical imaging are all are on some designer’s drafting board.

Arising from all of these CMOS imager benefits is a vast number of potential applications. A new cellular telephone standard being implemented within the next couple of years will have sufficient bandwidth to send images along with sound. Most all phone manufacturers are planning on implementing imagers into telephones; first addressing the insurance and realtor markets and then for everyday use. More and more toys will be implementing imagers. These will likely be of low-resolution format to keep data amounts small and will interface to television. The industrial and medical imaging markets will increase in size due to the lower cost of imaging and the decreased cost of image storage and processing. Of course, the traditional imaging markets of digital still cameras and video cameras will remain strong. It is even possible to integrate the entire camera on a
chip, where only an oscillator and power supply would be required with complete video (digital or analog) out of the chip. The only reason that has not been marketed yet is due to its limited market potential due to such specialization. All imager manufacturers at this time are concentrating on producing imagers that address a variety of applications.

4 Comparison of CCD and CMOS technologies

Much has been made in the past several years of the potential for CMOS imagers and of the impending demise of the incumbent image-sensing technology CCDs.

Strong claims by the proponents of a resurgent CMOS technology have been countered by equally forceful claims by CCD defenders. In a pattern typical of battling technologies (both with significant merits but also lacking maturity in some regards), users have become leery of performance representations made by both camps. Overly aggressive promotion of both technologies has led to considerable fear, uncertainty and doubt.

Imager basics

For the foreseeable future, there will be a significant role for both types of sensor in imaging. The most successful users of advanced image capture technology will be those who consider not only the base technology, but also the sustainability, adaptability and support. They will perform the best long term in a dynamic technology environment that the battle between CCDs and CMOS promises to deliver.

Both image sensors are pixilated metal oxide semiconductors. They accumulate signal charge in each pixel proportional to the local illumination intensity, serving a spatial sampling function.

When exposure is complete, a CCD transfers each pixel's charge packet sequentially to a common output structure, which converts the charge to a voltage, buffers it and sends it off-chip. In a CMOS imager, the charge-to-voltage conversion takes place in each pixel. This difference in readout techniques has significant implications for sensor architecture, capabilities and limitations.
Eight attributes characterize image sensor performance:

- **Responsivity**, the amount of signal the sensor delivers per unit of input optical energy. CMOS imagers are marginally superior to CCDs, in general, because gain elements are easier to place on a CMOS image sensor. Their complementary transistors allow low-power high-gain amplifiers, whereas CCD amplification usually comes at a significant power penalty. Some CCD manufacturers are challenging this conception with new readout amplifier techniques.

- **Dynamic range**, the ratio of a pixel’s saturation level to its signal threshold. It gives CCDs an advantage by about a factor of two in comparable circumstances. CCDs still enjoy significant noise advantages over CMOS imagers because of quieter sensor substrates (less on-chip circuitry), inherent tolerance to bus capacitance variations and common output amplifiers with transistor geometries that can be easily adapted for minimal noise. Externally coddling the image sensor through cooling, better optics, more resolution or adapted off-chip electronics cannot make CMOS sensors equivalent to CCDs in this regard.

- **Uniformity**, the consistency of response for different pixels under identical illumination conditions. Ideally, behavior would be uniform, but spatial wafer processing variations, particulate defects and amplifier variations create nonuniformities. It is important to make a distinction between uniformity under illumination and uniformity at or near dark. CMOS imagers were traditionally much worse under both regimes. Each pixel had an open loop output amplifier, and the offset and gain of each amplifier varied considerably because of wafer processing variations, making both dark and illuminated nonuniformities worse than those in CCDs. Some people predicted that this would defeat CMOS imagers as device geometries shrank and variances increased.

  However, feedback-based amplifier structures can trade off gain for greater uniformity under illumination. The amplifiers have made the illuminated uniformity of some CMOS imagers closer to that of CCDs, sustainable as geometries shrink.

  Still lacking, though, is offset variation of CMOS amplifiers, which manifests itself as
nonuniformity in darkness. While CMOS imager manufacturers have invested considerable effort in suppressing dark nonuniformity, it is still generally worse than that of CCDs. This is a significant issue in high-speed applications, where limited signal levels mean that dark nonuniformities contribute significantly to overall image degradation.

- **Shuttering**, the ability to start and stop exposure arbitrarily. It is a standard feature of virtually all consumer and most industrial CCDs, especially interline transfer devices, and is particularly important in machine vision applications. CCDs can deliver superior electronic shuttering, with little fill-factor compromise, even in small-pixel image sensors.

Implementing uniform electronic shuttering in CMOS imagers requires a number of transistors in each pixel. In line-scan CMOS imagers, electronic shuttering does not compromise fill factor because shutter transistors can be placed adjacent to the active area of each pixel. In area scan (matrix) imagers, uniform electronic shuttering comes at the expense of fill factor because the opaque shutter transistors must be placed in what would otherwise be an optically sensitive area of each pixel. CMOS matrix sensor designers have dealt with this challenge in two ways:

A nonuniform shutter, called a rolling shutter, exposes different lines of an array at different times. It reduces the number of in-pixel transistors, improving fill factor. This is sometimes acceptable for consumer imaging, but in higher-performance applications, object motion manifests as a distorted image.

A uniform synchronous shutter, sometimes called a nonrolling shutter, exposes all pixels of the array at the same time. Object motion stops with no distortion, but this approach consumes pixel area because it requires extra transistors in each pixel. Users must choose between low fill factor and small pixels on a small, less-expensive image sensor, or large pixels with much higher fill factor on a larger, more costly image sensor.

- **Speed**, an area in which CMOS arguably has the advantage over CCDs because all camera functions can be placed on the image sensor. With one die, signal and power trace distances can be shorter, with less inductance, capacitance and propagation delays. To date, though, CMOS imagers have established only modest advantages in this regard, largely because of early focus on consumer applications that do not demand notably high
speeds compared with the CCD's industrial, scientific and medical applications.

- **Windowing.** One unique capability of CMOS technology is the ability to read out a portion of the image sensor. This allows elevated frame or line rates for small regions of interest. This is an enabling capability for CMOS imagers in some applications, such as high-temporal-precision object tracking in a sub region of an image. CCDs generally have limited abilities in windowing.

- **Antiblooming,** the ability to gracefully drain localized overexposure without compromising the rest of the image in the sensor. CMOS generally has natural blooming immunity. CCDs, on the other hand, require specific engineering to achieve this capability. Many CCDs that have been developed for consumer applications do, but those developed for scientific applications generally do not.

- **Biasing and clocking.** CMOS imagers have a clear edge in this regard. They generally operate with a single bias voltage and clock level. Nonstandard biases are generated on-chip with charge pump circuitry isolated from the user unless there is some noise leakage. CCDs typically require a few higher-voltage biases, but clocking has been simplified in modern devices that operate with low-voltage clocks.

- **Reliability** Both image chip types are equally reliable in most consumer and industrial applications. In ultrarugged environments, CMOS imagers have an advantage because all circuit functions can be placed on a single integrated circuit chip, minimizing leads and solder joints, which are leading causes of circuit failures in extremely harsh environments.

CMOS image sensors also can be much more highly integrated than CCD devices. Timing generation, signal processing, analog-to-digital conversion, interface and other functions can all be put on the imager chip. This means that a CMOS-based camera can be significantly smaller than a comparable CCD camera.

The user needs to consider, however, the cost of this integration. CMOS imagers are manufactured in a wafer fabrication process that must be tailored for imaging performance. These process adaptations, compared with a nonimaging mixed-signal
process, come with some penalties in device scaling and power dissipation. Although the pixel portion of the CMOS imager almost invariably has lower power dissipation than a CCD, the power dissipation of other circuits on the device can be higher than that of a CCD using companion chips from optimized analog, digital and mixed signal processes. At a system level, this calls into question the notion that CMOS-based cameras have lower power dissipation than CCD-based cameras. Often, CMOS is better, but it is not unequivocally the case, especially at high speeds (above about 25-MHz readout).

The other significant considerations in system integration are adaptability, flexibility and speed of change. Most CMOS image sensors are designed for a large, consumer or near-consumer application. They are highly integrated and tailored for one or a few applications. A system designer should be careful not to invest fruitlessly in attempting to adapt a highly application-specific device for a use to which it is not suited.

CCD image sensors, on the other hand, are more general purpose. The pixel size and resolution are fixed in the device, but the user can easily tailor other aspects such as readout speed, dynamic range, binning, digitizing depth, nonlinear analog processing and other customized modes of operation.

Even when it makes economic sense to pay for sensor customization to suit an application, time to market can be an issue. Because CMOS imagers are systems on a chip, development time averages 18 months, depending on how many circuit functions the designer can reuse from previous designs in the same wafer fabrication process. And this amount of time is growing because circuit complexity is outpacing design productivity. This compares with about eight months for new CCD designs in established manufacturing processes. CCD systems can also be adapted with printed circuit board modifications, whereas fully integrated CMOS imaging systems require new wafer runs.

5 Compare the cost

One of the biggest misunderstandings about image sensors is cost.

Many early CMOS proponents argued that their technology would be vastly cheaper
because it could be manufactured on the same high-volume wafer processing lines as mainstream logic and memory devices. Had this assumption proved out, CMOS would be cheaper than CCDs.

However, the accommodations required for good electro-optical performance mean that CMOS imagers must be made on specialty, lower volume, optically adapted mixed-signal processes and production lines.

This means that CMOS and CCD image sensors do not have significantly different costs when produced in similar volumes and with comparable cosmetic grading and silicon area. Both technologies offer appreciable volumes, but neither has such commanding dominance over the other to establish untouchable economies of scale.

CMOS may be less expensive at the system level than CCD, when considering the cost of related circuit functions such as timing generation, biasing, analog signal processing, digitization, interface and feedback circuitry. But it is not cheaper at a component level for the pure image sensor function itself.

The larger issue around pricing, particularly for CMOS users, is sustainability. Many CMOS startups are dedicated to high-volume applications. Pursuing the highest-volume applications from a small base of business has meant that these companies have had to price below their costs to win business in commodity markets. Some start-ups will win and sustain these prices. Others will not and will have to raise prices. Still others will fail entirely.

CMOS users must be aware of their suppliers’ profitability and cost structure to ensure that the technology will be sustainable. The customer’s interest and the venture capitalist’s interest are not well-aligned: Investors want highest return, even if that means highest risk, whereas customers need stability because of the high cost of midstream system design change.

Increasingly, money and talent are flowing to CMOS imaging, in large part because of the high-volume applications enabled by the small imaging devices and the high digital processing speeds. Over time, CMOS imagers should be able to advance into
higher-performance applications.

For the moment, CCDs and CMOS remain complementary technologies — one can do things uniquely that the other cannot. Over time, this stark distinction will soften, with CMOS imagers consuming more and more of the CCD’s traditional applications. But this process will take the better part of a decade — at the very least.

6 Conclusion:

CCDs offer superior image quality and flexibility at the expense of system size. They remain the most suitable technology for high-end imaging applications, such as digital photography, broadcast television, high-performance industrial imaging, and most scientific and medical applications. Furthermore, flexibility means users can achieve greater system differentiation with CCDs than with CMOS imagers.

CMOS imagers offer superior integration, power dissipation and system size at the expense of image quality (particularly in low light) and flexibility. They are the technology of choice for high-volume, spaceconstrained applications where image quality requirements are low. This makes them a natural fit for security cameras, PC videoconferencing, wireless handheld device videoconferencing, bar-code scanners, fax machines, consumer scanners, toys, biometrics and some automotive in vehicle uses.

Sustainable cost between the two technologies is approximately equal. This is a major contradiction to the traditional marketing pitch of virtually all of the solely

7 Problems

1. Please briefly describe the working principle of a CCD image sensor

2. Please give a brief performance comparison of CCD and CMOS imagers.
References:


