On the Nonlinearity of Integrators in Continuous-Time Delta-Sigma Modulators

Adrian Leuciuc
State University of New York at Stony Brook
Department of Electrical and Computer Engineering
Stony Brook, NY 11794, USA

Abstract — In this communication the effect of nonlinearity of continuous-time integrators on the achievable signal to (noise + distortions) ratio SNDR of delta-sigma modulators is analyzed. It is shown that some topologies are less sensitive to the nonlinearities of the embodied integrators.

1 Introduction

Delta-Sigma modulation is one of the most popular ways to perform high-resolution data conversion of relatively low-bandwidth signals [1]. Although originally Delta-Sigma modulators for PCM and A/D conversion have been built using continuous-time circuitry, nowadays switched-capacitor implementations are dominating the market and scientific literature. The choice for either a switched-capacitor or a continuous-time realization is determined by several design aspects. Each of these two approaches has advantages and disadvantages. SC Delta-Sigma A/D converters can achieve high resolutions, are compatible with standard CMOS processes, and the frequency response of the noise shaping filter can be set very accurately since it depends only on capacitor ratios. On the other hand, CT implementations are less power hungry, are less prone to pick-up digital noise, are easy to drive from external sources, the errors of the S/H circuit is shaped by the loop filter and can operate at higher sampling frequencies. Among the factors limiting the maximum achievable SNR of CT Delta-Sigma modulators are: the linearity of the integrating stages, the clock jitter and the memory effect of the feedback DAC. The use of crystal oscillators and appropriate layout techniques can decrease the clock jitter, whereas the use of return-to-zero pulses can eliminate the memory effect of the feedback DAC. The linearity of the integrators can be improved by using high quality resistors in active-RC implementations, with the corresponding drawbacks: large die area, use of complex circuitry for tuning, increased manufacturing price. Therefore, high-performance and low-cost continuous-time delta-sigma modulators should use active transconductors to replace the passive resistors in the implementation of the noise-shaping filter.

2 Continuous-time integrators

2.1 Active-RC integrators

The fully-differential version of an active-RC integrator is depicted in Fig. 1a. From the point of view of integrated realization, active-RC filters have some drawbacks: the frequency range is reduced because of the presence of local feedback across the op-amp; the use of small value resistors requires large capacitors and increases the power consumption; small value capacitors request the use of large value resistors which are difficult to implement in standard processes; tuning can be achieved only by using programmable capacitance/resistance matrices.

2.2 OTA–opamp-C integrators

OTA–opamp-C integrators (Fig. 1b) have been derived from active-RC configurations by replacing the resistors with operational transconductance amplifiers (OTAs). This way, two of the disadvantages of the active-RC filters are eliminated: the need of large resistors and complex tuning. However, the reduced frequency range is preserved because of the local feedback and, additionally, the linearity achieved by these integrators is poor because of the nonlinear behavior of the input transconductors. MOSFET-C integrators are a particular case of OTA-opamp-C integrators in which the input transconductor is realized with MOSFETs operating in triode region as voltage controlled resistors.

2.3 G_m-C integrators

G_m-C integrators (Fig. 1c) have a feed-forward structure and therefore their operating frequency range is much higher compared to the two previous approaches. However, they have poor linearity and additional linearization

 0-7803-7150-X/01/$10.00@2001 IEEE

circuitry must be included. There are numerous papers describing different linearization techniques for both MOS and bipolar transconductors: cross-coupling of multiple differential pairs, adaptive biasing, source degeneration (using resistors or MOS transistors), shift level biasing, series connection of multiple differential pairs, combination of the above methods, pseudo-differential stages (using transistors in the triode region or in saturation).

From the linearity point of view, all continuous-time integrators depicted in Fig. 1 can be modeled by a cascade consisting of a nonlinear static operator (containing only odd order terms in the case of fully differential implementations) followed by an ideal integrator. When being part of a Delta-Sigma modulator, the integrators are driven by a signal containing both in-band components and out-of-band quantization noise. Depending on the amplitude of the in-band components driving the input of an integrating stage, its nonlinearity will affect more or less the signal to (noise+distortion) ratio of the modulator.

3 Topologies for delta-sigma modulators

In the following we will discuss only low-pass and single-loop topologies. Multi-stage cascaded topologies are not used for continuous-time implementations because of the difficulties in matching the parameters of the subsequent digital circuitry with the analog part. Since band-pass Delta-Sigma modulators can be obtained from low-pass prototypes by using simple frequency transformations, the results derived for the latter ones can be extended for the former.

Basically, most of the topologies for high-order single-loop Delta-Sigma modulators are using one of the two configurations shown in Fig. 2. Some other topologies are reported in literature [2], and also altered versions of the topologies presented in Fig. 2 (including local feedbacks to increase SNR) are often encountered in practice, but the two topologies in Fig. 2 will suffice to prove our claim. Although we are considering continuous-time modulators, we will analytically study their discrete-time equivalents. The qualitative results derived for the discrete-time systems are in complete agreement with the simulation results of the continuous-time ones, even though there is no exact one-to-one correspondence between the state variables of the discrete-time prototype and the continuous-time modulator.

Let us assume all the integrators in the topologies depicted in Fig. 2 are with delay. This will simplify our analysis and the results can be easily extended to the case when the modulator contains delay-free integrators as well. Our aim is to compute the signal and noise transfer functions corresponding to each of the state variables

$$G_k = \frac{X_k}{U}, H_k = \frac{X_k}{E} \tag{1}$$

where U is the input of the modulator, E is the quantization noise, and X_k are the state variables (the outputs of the integrators).

3.1 The CIFB topology

For the CIFB topology (Fig. 2a) we obtain

$$Y(z) = G(z)\,U(z) + H(z)\,E(z) \tag{2}$$

where

$$G(z) = \frac{a_1}{P(z)}; H(z) = \frac{(z-1)^N}{P(z)} \tag{3}$$

The denominator P(z) is given by

$$P(z) = (z-1)^N + \sum_{i=1}^{N} a_i (z-1)^{i-1} \tag{4}$$

and the feedback coefficients are computed in such a manner to ensure a maximum flat frequency response for the noise transfer function and a maximum gain guaranteeing stability. The state variables are

$$X_k(z) = \frac{a_1 P_k(z)}{P(z)} U(z) - \frac{(z-1)^{N-k}}{P(z)} E(z) \tag{5}$$

where

$$P_k(z) = (z-1)^{N-k} + \sum_{i=k}^{N} a_i (z-1)^{i-k-1} \tag{6}$$

Each state variable will contain some filtered quantization noise plus a filtered version of the input signal. In the case of CIFB topology, all signal transfer functions $G_k(z)$ are low-pass ones, whereas $H_k(z)$ are of high-pass type, removing less and less noise going from the first stage to the last one. Therefore, the first integrator will have the largest input signal component and the minimum amount of quantization noise, while the last one will contain a small part of the input signal and the maximum amount of noise. Since the output of an integrator represents the input of the subsequent integrating stage, it follows that the linearity of the first integrating stages is more critical than the linearity of the final ones.

3.2 The CIFF topology

For the CIFF topology, depicted in Fig 2b, the noise transfer function has the same expression as in (3), but the signal transfer function is

$$G(z) = 1 - H(z) \tag{7}$$

The state variables are

$$X_k(z) = \frac{(z-1)^{N-k}}{P(z)}(U(z) - E(z)) \qquad (8)$$

The signal and noise transfer functions are identical, $G_k(z) = H_k(z)$, being high-pass filters with less and less attenuation in the signal band going from the first stage to the last one. Therefore, the first state variable will contain only a very small component of the input signal (this one being almost totally removed) and a large amount of filtered quantization noise. The nonlinearity of the second integrator will not introduce in-band components, but only out-of-band distortions. The last integrator will introduce the largest amount of in-band distortions, but these will be shaped by the loop filter. For this topology, as it will be shown in the next section, only the linearity of the input integrating stage is critical, all others not being detrimental to SNDR.

4 Simulation results

The design of a continuous-time Delta-Sigma modulator starts from a discrete-time prototype and applying some discrete-time to continuous-time transformations. One can use a state space approach [3], the impulse response invariance [4], [5],or pole-zero mappings. Two fifth order continuous-time Delta-Sigma modulators have been designed with the two topologies depicted in Fig. 2 and using the approach presented in [3]. In order to make an unbiased comparison for all integrating stages, the modulator has been scaled to have the equal signal swings at the output of all integrators and equal to the maximum input level guaranteeing stability. Thus, all integrators are driven by equal amplitude signals. Using a cubic type nonlinearity for the integrators

$$f(x) = x - n \cdot x^3, \qquad (9)$$

behavioral simulations have been carried out for the two topologies of fifth-order continuous-time Delta-Sigma modulators. Figure 3 shows the drop in SNDR (OSR=64) as a function of the coefficient n when the nonlinearity affects each integrator separately. As predicted, for the CIFB topology, the linearity of integrators is important for all stages (since G_k are low-pass transfer functions), the most critical stage being the first one, driven by the input signal itself. The second integrator requires almost the same linearity as the first one, and the specifications for the subsequent stages can be eased as one approaches the quantizer. For the CIFF topology the influence of the input integrator nonlinearity is quantitatively the same as in the case of CIFB topology, but the linearity of all other stages is not affecting SNDR to such great extent. Actually, the nonlinearity of the final three integrators have a negligible effect on SNDR.

5 Conclusions

The analysis presented herein has shown that the nonlinearity of integrating stages affects differently the performance of a Delta-Sigma modulators, depending on the chosen topology. This result is especially significant for the case of continuous-time implementations that are more affected by the nonlinearity of integrators. From the linearity point of view, the most advantageous topology is the one depicted in Fig. 2b because it imposes easier constraints on the integrating stages. However, additional factors should be considered in the design of a Delta-Sigma modulator. For example, for a fifth order Delta-Sigma modulator, the unit gain frequency of the first integrator is approximately five times higher for CIFF topology, compared to CIFB. Considering a MOS implementation (for which the transconductance of a differential pair depends on the square-root of the tail current), it follows the power dissipation in the first integrator can be almost 25 times larger for the CIFF configuration. Since the first stage is already taking most of the power consumption because of the noise and linearity requirements, CIFB topology could be a better choice, even though one has to use more linear integrating stages to achieve the same SNDR.

References

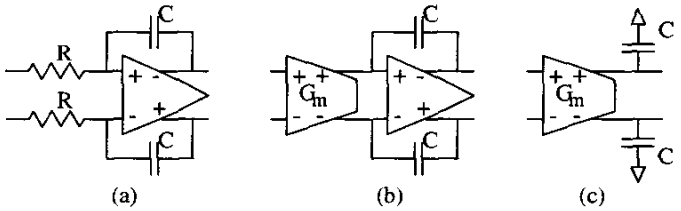
[1] S.R. Norsworthy, R. Schreier, and G.C. Temes (eds.), "Delta-Sigma Data Converters: Theory, Design, and Simulation", New York: IEEE Press, 1997.

[2] W.L. Lee and C.G. Sodini, "A Topology for Higher Order Interpolative Coders", Proc. of ISCAS'87, pp. 459-462.

[3] R. Schreier and B. Zhang, "Delta-Sigma Modulators Employing Continuous-Time Circuitry", IEEE Trans. Circuits and Syst.-I, vol. 43, no. 4, April 1996, pp. 324-332.

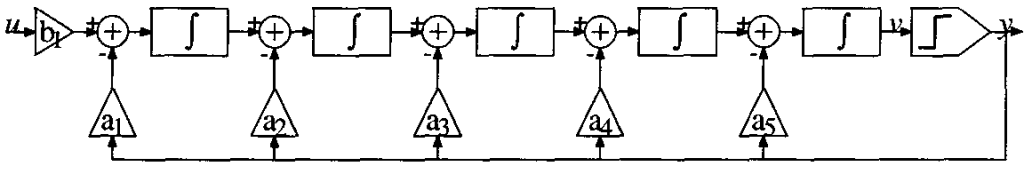
[4] O. Shoaei, "Continuous-Time Delta-Sigma A/D Converters for High Speed Applications", Ph.D. dissertation, Carleton Univ., Ottawa, Canada, 1996.

[5] J.A. Cherry and W.M. Snelgrove, "Excess Loop Delay in Continuous-Time Delta-Sigma Modulators", IEEE Trans. Circuits and Syst.-II, vol. 46, no. 4, April 1999, pp. 376-389.

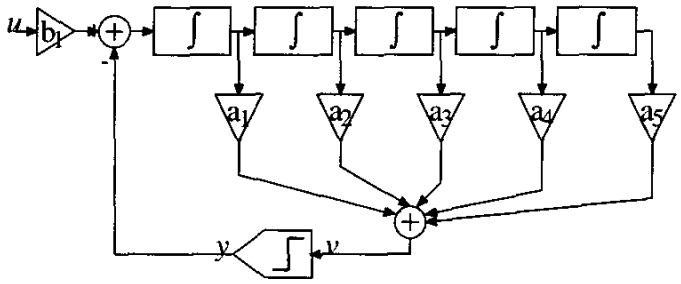


(a) (b) (c)

Fig. 1. Continuous-time integrators

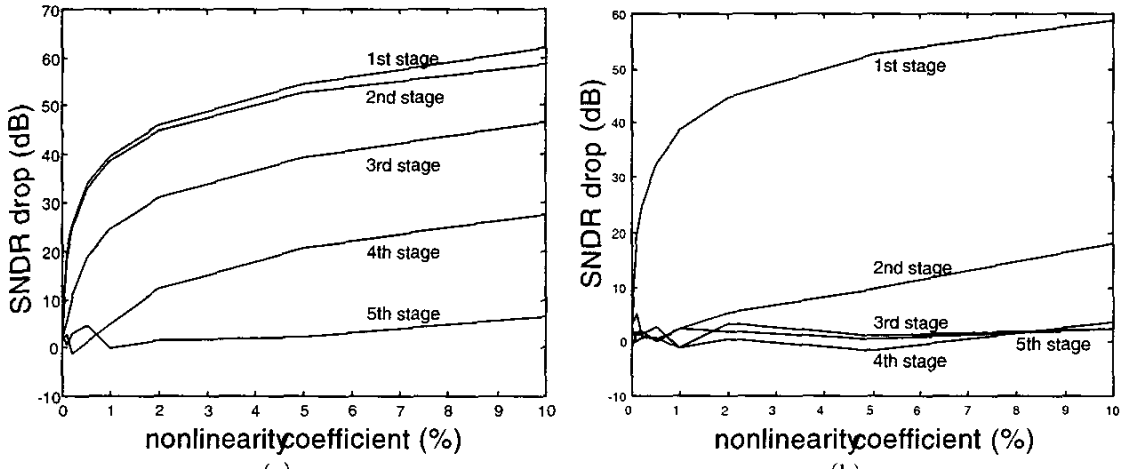


(a)



(b)

Fig. 2. Topologies for single-loop Delta-Sigma modulators: (a) Cascade of integrators with distributed feedback CIFB; (b) Cascade of integrators with feed-forward summation CIFF.



(a) (b)

Fig. 3. The effect of nonlinearity of integrating stages for the (a) CIFB topology and (b) CIFF topology.