A WIDE LINEAR RANGE LOW-VOLTAGE TRANSCONDUCTOR

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ABSTRACT

This paper presents a wide linear range transconductor based on the differential pair with emitter/source degeneration. The proposed circuit can be implemented in both bipolar and CMOS technology. The transconductor exhibits high linearity that is achieved by forcing a constant current through the main transistors in the differential pair and collecting the output current by means of two additional transistors and two current mirrors. Simulation results are presented for a CMOS implementation operating at a 1.8V supply voltage.

1. INTRODUCTION

Operational transconductance amplifiers (OTAs or transconductors) are basic building blocks in high-frequency continuous-time filters and continuous-time delta-sigma modulators. Compared to op-amp based integrator topologies (active-RC, MOSFET-C), the OTA-C (or $G_m - C$) approach has the advantage of a feed-forward structure and therefore of a higher frequency operating range. The main drawback of OTA-C filters is the nonlinearity of transconductors that introduces distortions at the outputs of integrators. Several techniques to improve the linearity performance of both bipolar and MOS transconductors have been proposed in the literature. Roughly, these methods can be grouped in two classes: (i) compensation of transistor nonlinearity with other transistors of the same type; (ii) use of passive resistors to achieve the desired linearity. Transistor-only linearization methods include: cross-coupling of multiple differential pairs [1], [2], [3], adaptive biasing [1], [4], source degeneration using MOS transistors [5], shift level biasing [7], and pseudo-differential stages (using transistors in the triode region or in saturation) [8], [9]. However, for all these techniques the reported transconductor linearity is limited to 40-60 dB. Nevertheless, applications like delta-sigma modulators for high resolution A/D converters, and filters for HDTV require better linearity, corresponding to more than 10-b. Such a linearity performance can be achieved by using resistor-based transconductors [10]-[15]. This paper describes the implementation of a wide linear range resistor-based transconductor capable of low-voltage operation.

2. LINEAR TRANSCONDUCTORS USING RESISTORS

Most of the resistor-based linear transconductors are based on the simple differential-pairs with resistive emitter/source degeneration (Fig. 1). These circuits are described by

$$v_i - Ri_o = v_{BE1} - v_{BE2} = \Delta v_{BE}, \qquad (1)$$

respectively

$$v_i - Ri_o = v_{GS1} - v_{GS2} = \Delta v_{GS}, \qquad (2)$$

where $v_i = v_{i1} - v_{i2}$. The right side term in (1)-(2) characterizes the nonlinearity of the transconductors. Ideally, one wants to have the output current set only by resistor R. Therefore, one should satisfy $\Delta v_{BE} = 0$, respectively $\Delta v_{GS} = 0$.

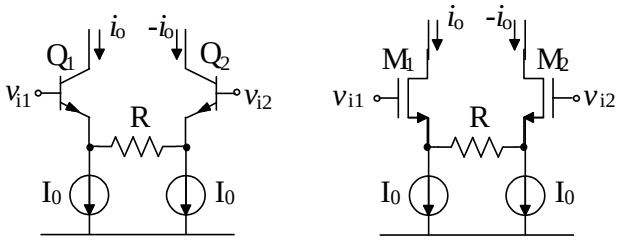

Figure 1. Differential pairs with emitter/source resistive degeneration

The linearity problem is more critical in the MOS case because of the quadratic dependence of the gate-to-source voltage on the drain current. This is the reason why throughout this communication one emphasizes the MOSFET-based circuits, but the reader should be aware that similar topologies are valid using bipolar technology. One way to achieve the above conditions is to use the topologies proposed in [11], [15]

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and based on the configuration depicted Fig. 2(a). In this figure the two additional op-amps will force the input voltage to be equal to the voltage across resistor R which will set the output current i_o.

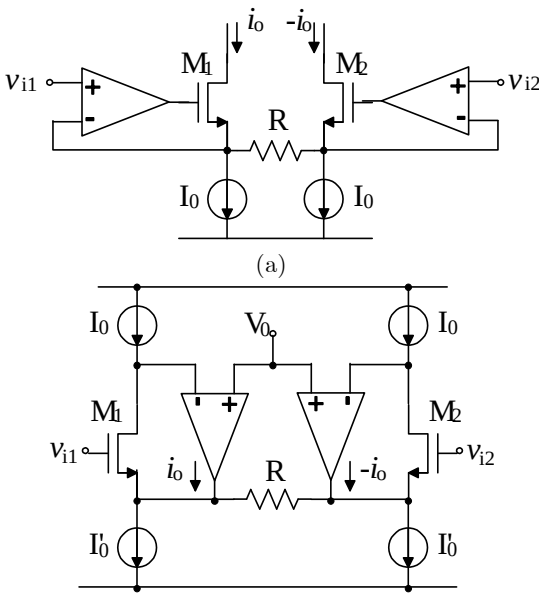

Figure 2. Two possibilities of improving the linearity of the circuits in Fig. 1.

The alternative solution proposed in this communication is depicted in Fig. 2(b). One uses again two additional op-amps, but this time their role is to ensure constant currents I_0 flowing through the differential pair transistors. The output currents are available at the outputs of the op-amps and one can find several different circuit configurations to deliver these currents to the load, as it will be shown in the next section. V_0 sets the voltage at the high impedance nodes at the drains of transistors $M_1 - M_2$ and the tail current sources I_0' may be different from I_0 to supply possible biasing currents for the outputs of op-amps. The op-amps can be replaced by operational transconductance amplifiers (OTAs) without significantly changing the operation of the circuit. However, one has ensure that the product $G_{OTA}R$ is large enough in order to maintain an approximately constant voltage at the drains of transistors $M_1 - M_2$. Actually, as shown in the next section, the proposed transistor-level implementations of the topology in Fig. 2(b) are using simple transconductors instead of op-amps.

3. CIRCUIT IMPLEMENTATION

The most straightforward realization of the topology shown in Fig. 2(b) is to use as op-amps two fully differential emitter/source coupled stages and to deliver the output currents from their unused, high resistance output terminals (Fig. 3). Nevertheless, a simpler solution is to use single ended amplifiers and current mirrors to supply the output currents. One such possible realization has been proposed in [10] and it is shown in Fig. 4(a). The amplifiers are implemented with transistors $M_3 - M_5 - M_{11}$, respectively $M_4 - M_6 - M_{12}$. The minimum supply voltage allowed for this circuit is given by $2V_{GS} + V_{DS(sat)} = 2V_T + 3V_{DS(sat)}$. The bipolar version of the circuit depicted in Fig. 4(a) has been reported in [12].

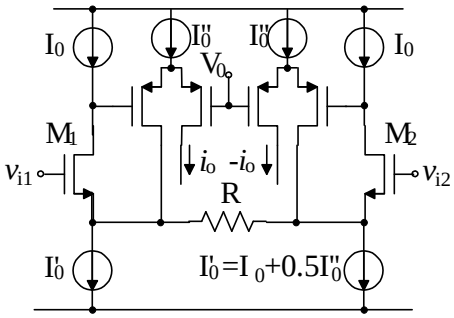

Figure 3. A straightforward realization of the transconductor in Fig. 2(b).

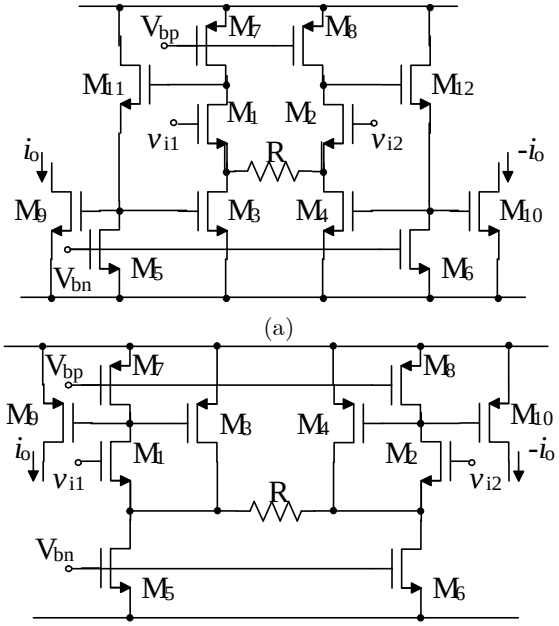

Figure 4. Two possible implementations of the transconductor in Fig. 2(b).

The author proposes a more compact implementation, capable of operating at even lower supply voltages, and depicted in Fig. 4(b). In this case the amplifiers are implemented using a single transistor in a common source configuration (M_3 and M_4) and the minimum supply voltage ensuring all transistors operating in saturation is $V_{GS}+2V_{DS(sat)} = V_T+3V_{DS(sat)}$.

A similar BiCMOS implementation has been previously reported in [16].

3.1. Frequency response and stability

As any system with feedback, the circuit in Fig. 4(b) may have stability problems. The open-loop circuit is characterized by a low-frequency gain

$$T = \frac{g_{m1} g_{m3} R^* R}{(2 + g_{m1} R)},$$

three poles set by the time constants

$$\tau_1 = R^* C^*, \tau_2 = \frac{C_{gs1} R}{2 + g_{m1} R}, \tau_3 = (C_{gd3} + C_{gd5}) \frac{R}{2},$$

and two high frequency right half plane zeros. In the above expressions $R^* = r_{o7} || r_{o1} \left(1 + g_{m1} \frac{R}{2}\right)$ and C^* is the capacitance at the drain of M_1. The dominant pole set by τ_1 can be made small enough by design to guarantee a 60^0 phase margin.

3.2. Noise analysis

The power spectrum density of the input referred noise voltage results

$$S_{v_{in}}(f) = 4kTR + \frac{R^2}{2} \left(\frac{4}{(g_{m1} R)^2} S_{i_1}(f) + S_{i_3}(f) + \right.$$

$$\left. S_{i_5}(f) + \left(\frac{2 + g_{m1} R}{g_{m1} R} \right)^2 S_{i_7}(f) + S_{i_9}(f) + S_{i_{load}}(f) \right)$$

where $S_{i_k}(f)$ is the power spectrum density of the drain noise current of transistor M_k:

$$S_{i_k}(f) = \frac{8}{3} kT g_{mk} + \frac{K_f}{f} \frac{g_{mk}^2}{(WL)_k C_{ox}^2}$$

It can be easily seen that one can minimize the noise contribution of $M_{1,2}$ and $M_{7,8}$ by making the product $g_{m1} R$ as large as possible. For a given R and input linear range (that sets the gate-to-source overdrive voltage of $M_{1,2}$) this will increase the power consumption and one has to make a trade-off dissipated power/noise.

4. SIMULATION RESULTS

The circuit in Fig. 4(b) have been designed using the TSMC CMOS $0.25 \mu m$ process and simulated in Hspice using a single 1.8V supply voltage. To maximize the linear range, all MOSFETs are operating in the moderate inversion region with gate-to-source overdrive voltages in the range of (100-130)mV. When using NMOS input devices, the optimum input common mode voltage is around 1.1V. Figure 5 shows the simulated transconductance for different source degeneration resistor values. There is a small difference between the predicted value of the transconductance ($G_m = 1/R$) and the obtained one. The reason for this is that the body effect of $M_{1,2}$ has been neglected in all the above calculations. Considering the body effect, the small signal transconductance of the circuit in Fig. 4(b) is

$$G_m = \frac{g_{m1}}{g_{m1} + g_{mb1}} \frac{1}{R} = \frac{2\sqrt{2\phi_f + V_{SB1}}}{2\sqrt{2\phi_f + V_{SB1}} + \gamma} \frac{1}{R}$$

which is in a good agreement with the simulation results. The ideal value of the designed transconductance can be obtained by using input PMOS devices with their bodies and sources tied together.

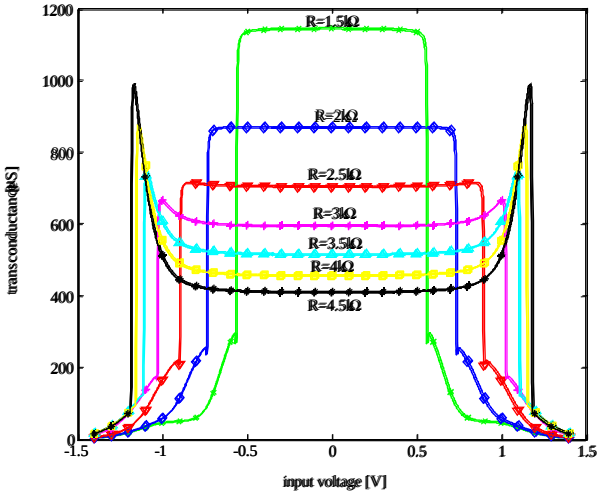

Figure 5. Simulated transconductance

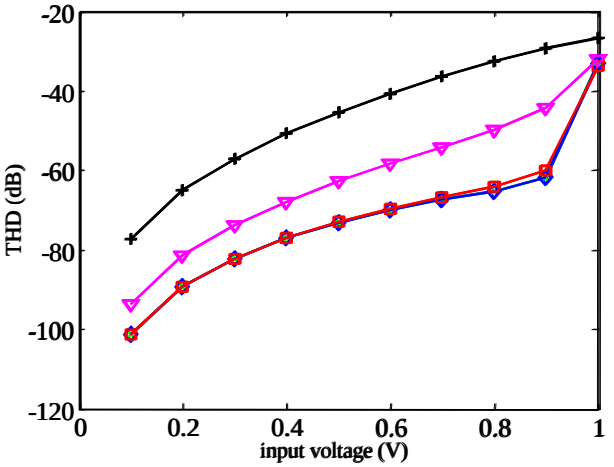

Figure 6. Simulated THD: × - 1kHz; ◇ - 10kHz; □ - 100kHz; ▽ - 1MHz; + - 10MHz

In Fig. 6 the simulated THD as a function of the input signal amplitude is plotted for different frequencies. THD is less than -60dB for 1Vp-p input up to 1MHz and for 1.8Vp-p input up to 100kHz. The rather poor linearity of the proposed circuit for frequencies higher than a couple of hundreds of kHz is due to the large nonlinear capacitances present at the drains of transistors $M_{1,2}$.

5. CONCLUSIONS

A novel transconductor with wide linear range and operating at low supply voltages is presented. The proposed transconductor uses a passive resistor to achieve high linearity. Compared to transistor-only transconductors that can be usually easily tuned, resistor-based transconductors necessitate more complex tuning circuitry (e.g. translinear loops, electronically controlled current mirrors, arrays of passive devices). However, by replacing the resistor with MOSFETs operating in the triode region [6] one can still achieve good linearity while adding the advantage of simple tuning technique. The proposed transconductor can be used in continuous-time filters with tough linearity requirements or in high SNDR continuous-time delta-sigma modulators.

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