Nonlinear Stabilization Techniques for ΔΣ Modulators: A Comparison

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Abstract

Three nonlinear stabilization techniques for higher-order, single-loop and single-bit ΔΣ modulators are presented in this communication. The performances of the three methods are analyzed for the topology with distributed feedback [1], but the techniques can be extended to other single-loop topologies. The stabilization mechanism is activated only if the modulator overload is detected. Thus, the peak SNR achievable with a modulator without such stabilization circuitry is preserved. The performances of the presented methods are compared by measuring the SNDR of the stabilized modulators.

1 Introduction

Higher-order, single-loop and single-bit ΔΣ modulators are known for their instability when driven by large input signals, with amplitudes close to the reference voltage of the feedback D/A converter. The higher the order of the modulator, the lower is the maximum admissible input guaranteeing stability. The lack of rigorous analytical results on the stability of modulators of order three and higher determined the designers to use intuitive techniques for stabilizing them. There are several nonlinear stabilization methods used for ensuring the global stability of higher-order modulators: bounding the state variables values (clipping the output of integrators) [2], resetting the integrators when oscillations are detected [3], addition of local feedback signals at the input of integrators [4, 5]. The first two methods introduce large distortions in the output modulated signal, especially when the input signal continuously overloads the modulator for an extended period of time. The modulators stabilized using the method presented in [4, 5] generate a multi-bit output signal, making thus the subsequent digital filtering more complex. In this communication we present some new or modified techniques for stabilizing the higher-order, single-loop and single-bit ΔΣ modulators. The proposed goal to be achieved is the maximization of the signal to (noise + distortions) ratio, SNDR, when the modulator is overload by large amplitude input signals.

2 State space description of ΔΣ modulators

To justify the use of the three nonlinear stabilization techniques to be presented in section 3, let us write the state equation for the general structure of a discrete-time, normalized (V_{ref}=1V), single-bit ΔΣ modulator (Figure 1)

$$\begin{aligned} \boldsymbol{x}[k+1] &= \boldsymbol{A}\,\boldsymbol{x}[k] + \boldsymbol{b}_1 u[k] - \boldsymbol{b}_2 v[k] \\ v[k] &= sign(y[k]) = sign\left(\boldsymbol{c}^T \boldsymbol{x}[k] + d\,u[k]\right), \end{aligned} \qquad (1)$$

where $\boldsymbol{x}[k]_{Nx1}$ is the state vector, $\boldsymbol{A}_{NxN}$ is the state matrix, $\boldsymbol{b}_1$, $\boldsymbol{b}_2$, and $\boldsymbol{c}$ are Nx1 vectors, d is a scalar. Since a continuous-time ΔΣ modulator can be transformed into a discrete-time equivalent [6], we will consider in the following only the discrete-time case.

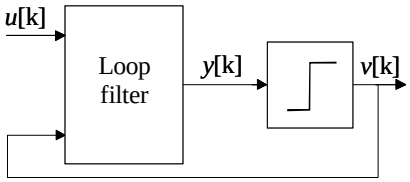

Figure 1. General single-bit ΔΣ modulator

The analysis of the global dynamics of such a nonlinear system is difficult to perform. It is much easier to consider the linear maps in the two partitions of the phase space corresponding to the two possible values of the output variable $v[k]$

$$\boldsymbol{x}[k+1] = \boldsymbol{A}\,\boldsymbol{x}[k] + \boldsymbol{b}_1 u[k] - \boldsymbol{b}_2 \cdot (\pm 1). \qquad (2)$$

The difference equation (2) can be easily solved using the **Z** transform. Let us consider k=0 the time instant when the phase orbit crosses the boundary between the two phase space partitions, and $\boldsymbol{x}_0=\boldsymbol{x}[0]$ the initial condition for the corresponding linear map. We have

$$\boldsymbol{X}(z) = (z\boldsymbol{I} - \boldsymbol{A})^{-1}\left(z\boldsymbol{x}_0 + \boldsymbol{b}_1 U(z) - \boldsymbol{b}_2 \cdot \left(\pm \frac{z}{z-1} \right) \right), \qquad (3)$$

where $\boldsymbol{X}(z)=[X_1(z)\ X_2(z)\ \ldots\ X_N(z)]^T$, $X_n(z)=\mathbf{Z}\{x_n[k]\}$, n=1,..., N.

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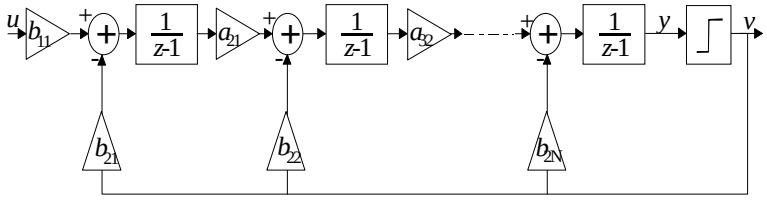


Figure 2. Cascade of integrators with distributed feedback topology

For simplicity, we will restrict the discussion to the topology of cascade of integrators with distributed feedback (Figure 2), but the results can be extended to other loop filter configurations. In this case, due to the particular form of the state matrix $\boldsymbol{A}$ (lower triangular, with ones on the main diagonal), the denominator of each component of the vector $\boldsymbol{X}(z)$ contains factors of the form $(z-1)^i$, i=1, ..., N+1. This means that all the positive terms in the numerator of $X_n(z)$ will determine an increase in $x_n[k]$, whereas the negative terms will tend to decrease the state variables. The modulator becomes overload when the initial condition $\boldsymbol{x}_0$ and input $u[k]$ have all large values of the same sign, determining a further increase in the absolute value of the state variables. The negative feedback is not able anymore to balance this behavior, but only after a rather long period. The effect is an output containing long strings of bits 1 or 0, a sign for instability.

From the discussion above we can derive two procedures for stabilizing the modulator: when overload is detected, increase the negative feedback, or decrease the influence of the forward paths. We can detect when the modulator is overload looking only at the output of the loop filter, before the quantizer (global overload detection), or we can check all integrator outputs (local overload detection). The numerous simulations that have been carried out proved that nonlinear stabilization based on local overload detection has better performances compared to the one using the global overload detection.

3 Stabilization techniques

3.1. Method 1: zeroing the integrator input

This method consists in switching to ground, when overload is detected, the integrator inputs connected to the outputs of previous integrators or to the input signal (Figure 3a). Thus, the difference equation describing the functioning of the integrator becomes

$$x_n[k+1] = x_n[k] - b_{2n} v[k] \qquad (4)$$

and taking into account that during overload the state variable has the same polarity as the output signal $v[k]$, the integrator output will return shortly within the normal operation bounds. The method is extremely simple to implement, especially in a switched capacitor realization. However, since there are no parameters to control the stabilization mechanism, the generated distortions could be large.

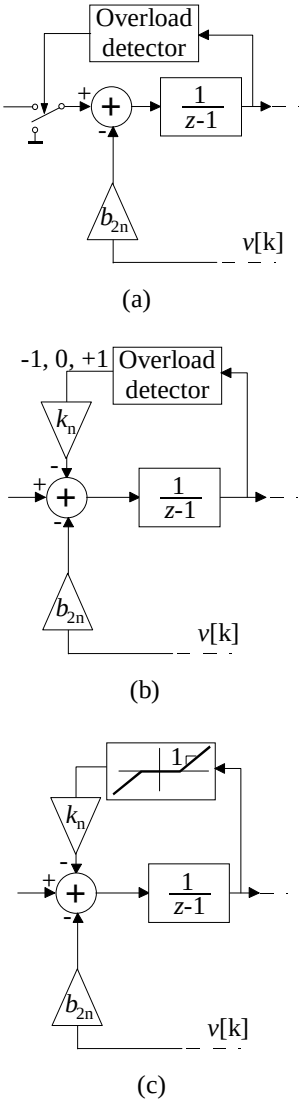


Figure 3. Block diagrams illustrating the nonlinear stabilization techniques: (a) method 1; (b) method 2; (c) method 3.

3.2. Method 2: adding local feedback signals

This technique, depicted in Figure 3b, was proposed in [4] and further improved in [5]. Upon the detection of integrator overload, an additional negative feedback signal is applied at its input, determining the output to return within the normal operation bounds. In [4, 5] the modulator was augmented with a digital cancellation circuitry, generating a multi-bit output: 9-bit in [4], 4-bit in [5], respectively. The parameters associated with the stabilization blocks were chosen in such a manner to reduce the complexity of the digital cancellation circuitry. Without this cancellation, the distortions of the stabilized, single-bit modulator can be very large. Furthermore, good matching between the parameters of the analog and digital blocks is required, as in the case of cascaded ΔΣ modulators. The approach presented in this communication optimizes the parameters of the stabilization circuitry, k_n, in order to achieve the maximum SNDR. The obtained performances are comparable with the ones obtained in [4], but worse than the results reported in the improved modulator of [5].

3.3. Method 3: using nonlinear feedback

This approach can be seen as a generalization of the nonlinear stabilization method based on bounding the integrator outputs. Each integrator is augmented with a nonlinear block in the feedback path, as is shown in Figure 3c. Instead of using a hard limiter, the slopes of the feedback nonlinearity are finite, equal to k_n for the n-th integrator. Again, we have to optimize the parameters k_n in order to maximize the SNDR.

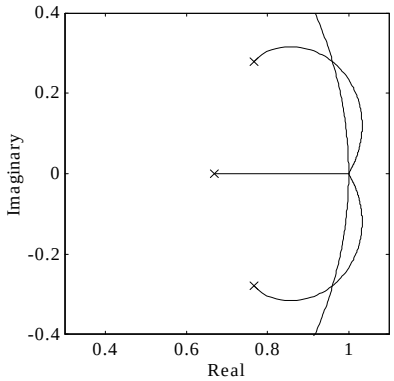
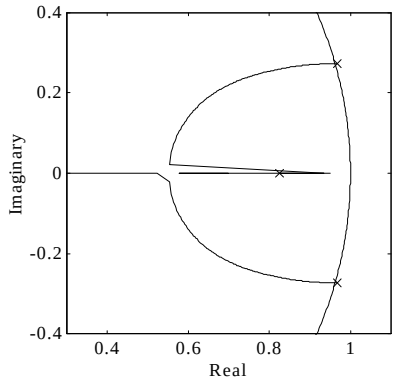


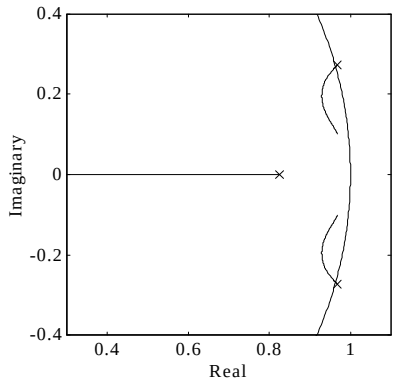
Figure 4. Root locus at the variation of quantizer gain

The efficiency of the last two methods can be also justified if we model the one-bit quantizer using the description function, associating to it a signal dependent gain [7]. In this case, increasing the level at the input of the quantizer, its gain will decrease and the poles of the noise transfer function may move outside the unit circle. This behavior is depicted in Fig. 4 where the root locus at the variation of quantizer gain from 1 to zero is plotted in the case of a third order modulator.

The last two stabilization methods can be seen as introducing controlled leakage in the integrators, upon detection of overload. Considering that overload detection corresponds to the limit of stability (poles on the unit circle), the effect of integrators' leakage over the root locus is shown in Fig. 5, for the same third order modulator. It can be seen that the poles are moved inside the unit circle, stabilizing the modulator



(a)



(b)

Figure 5. Root locus at the variation of integrators leakage, quantizer gain=0.3: (a) 2nd integrator; (b) 3rd integrator

4 Simulation results and conclusions

The three nonlinear stabilization methods described in section 3 have been tested in the case of a third order ΔΣ modulator with the topology of Figure 2. The shaping filter has a noise transfer function of Butterworth type with a maximum gain of 1.5 [8, 9] that guarantees stability for inputs with amplitudes smaller or equal to

approximately 0.75. The integrator gains have been scaled to obtain maximum dynamic range. Since we were not able to derive a rigorous method for computing the optimum parameters of the stabilization circuitry ensuring the maximum SNDR, numerous simulations have been carried out in order to determine these values. The results are summarized in Figure 4 where the simulated SNDR for a third order modulator, without and with stabilization circuitry using the three methods, is plotted. The oversampling ratio is 64 and the modulator has been driven by a sinusoidal input with frequency $f_s/256$, f_s being the sampling rate. The following parameters have been used: method 2: $k_1=0$, $k_2=0.08$, $k_3=0.6$; method 3: $k_1=0$, $k_2=1.1$, $k_3=0.68$. It can be easily observed that the peak SNR of the original modulator is preserved by all three stabilization methods. The droop in SNDR for large amplitude input signals is larger for method 1 and smaller for the last one. Nevertheless, the simplicity of the first method can compensate this disadvantage.

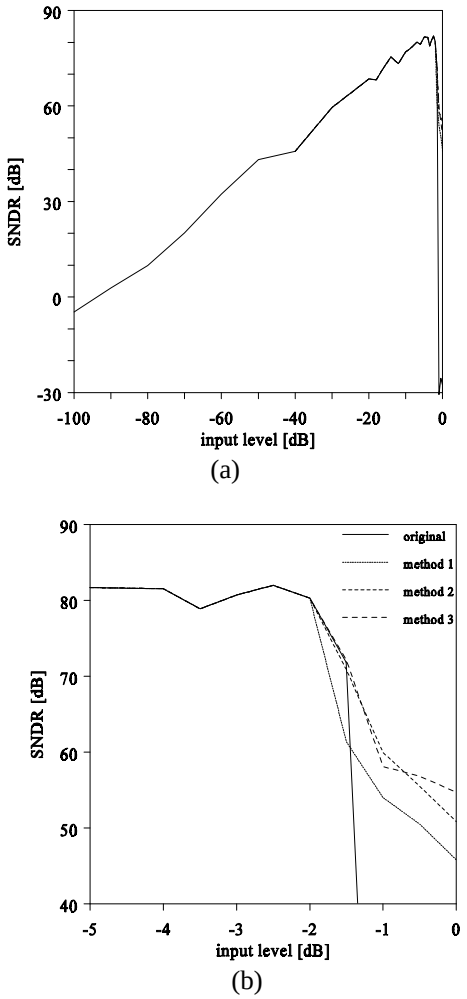


Figure 6. SNDR for the original and stabilized third-order ΔΣ modulator: (a) entire plot; (b) detail.

Further work should be performed in this area. In the absence of analytical expressions for computing the parameters of the stabilization circuitry to maximize SNDR, one should derive some numerical algorithms to solve this problem. Furthermore, a prediction mechanism of possible instability should be developed and the stabilization circuitry to be activated in a smooth manner.

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