A Linear MOS Transconductor Using Source Degeneration and Adaptive Biasing

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***Abstract*—This paper presents a new configuration for linear MOS voltage-to-current conversion (transconductance). The proposed circuit combines two previously reported linearization methods [1], [2]. The topology achieves 60-dB linearity for a fully balanced input dynamic range up to 1 V_{pp} at a 3.3-V supply voltage, with slightly decreasing performance in the unbalanced case. The linearity is preserved during the tuning process for a moderate range of transconductance values. The approach is validated by both computer simulations and experiments.**

***Index Terms*—Continuous-time filters, MOS transconductors.**

I. Introduction

Integrated analog filters can be realized using two different approaches: discrete-time (switched-capacitor or switched-current) and continuous-time implementations. The switched-capacitor and switched-current filters are limited to low frequency applications due to the sampling process. Continuous-time filters, on the other hand, have a significant speed advantage over discrete-time counterparts because no sampling is required.

There are three main techniques to implement integrated continuous-time filters: active-*RC*, MOSFET-C, and G_m-C. Active-*RC* configurations use op-amps, and resistors and capacitors as passive frequency-determining components. They present very good linearity, but usually require large die area for resistors and/or capacitors, the tuning can be achieved only in a discrete manner by using arrays of passive components, and the large value resistors can introduce substantially thermal noise.

Another class of continuous-time filters is derived from classical active-*RC* filters and uses MOS field-effect transistors (MOSFETs), capacitors, and op-amps. They are thus referred to as MOSFET-C active filters [3], [4]. These implementations have poor linearity due to the nonlinear characteristic of the MOS transistors. Although the linearity can be improved by using multiple cross-coupled transistors [5], the input dynamic range is reduced in order to keep the MOSFETs in the triode region. For example, in [6] such an integrator achieves THD of only -40 dB for $0.7V_{\rm rms}$ at a single 5-V supply.

The use of transconductors and capacitors to implement integrators is another technique to realize continuous-time filters. The G_m-C configurations [7], [8] have better frequency response compared to active-RC and MOSFET-C realizations due to the absence of local feedback around the active elements. They have also electronic tuning capability, but are characterized by a rather poor linearity. Therefore, additional circuitry is needed to linearize the transfer characteristic of a transconductor.

Since G_m-C configurations have better frequency response and usually wider tuning range, they are nowadays among the most popular approaches for implementing integrated continuous-time filters. Several circuit techniques have been proposed in literature to improve the linearity of bipolar and MOS transconductors. In this communication we will refer only to MOS transconductors, a good survey on most of the linearization techniques being given in [9]. The linearization methods include: cross-coupling of multiple differential pairs [2], [10], [11], adaptive biasing [2], [12], source degeneration (using resistors or MOS transistors) [1], [13], [14], shift level biasing [15], series connection of multiple differential pairs [16], and pseudodifferential stages (using transistors in the triode region or in saturation) [17], [18]. This paper presents an improved linear MOS transconductor that uses both the adaptive biasing and source degeneration approaches. Section II reviews these two linearization techniques and the configuration of the newly proposed transconductor is described. Several comparative simulation results are presented in Section III. The novel linear transconductor has been fabricated in a 0.35-μm process, using a single 3.3-V supply voltage. Experimental results are included for comparison to the simulation results. Some final conclusions are presented in Section IV.

II. Circuit Topologies for Linear MOS Transconductors

In this section, we will first review three linearization techniques previously reported in literature. The first one is the MOS differential pair with resistive source degeneration. The second one was introduced in [1] and consists of a MOS differential pair with source degeneration using MOS transistors. The third one [2] makes use of an adaptive biasing current source to cancel the nonlinearity of the simple MOS differential pair. The advantages and disadvantages of these three techniques will be discussed. Then the new linear MOS transconductor is introduced.

A. MOS Transconductors With Resistive Source Degeneration

In the following analysis we will consider perfectly quadratic i–v characteristics for the MOS transistors in the saturation re-

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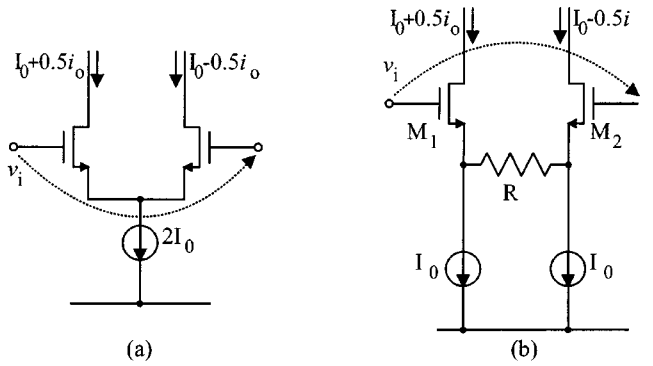

Fig. 1. (a) Simple differential MOS transconductor. (b) MOS transconductor with resistive source degeneration.

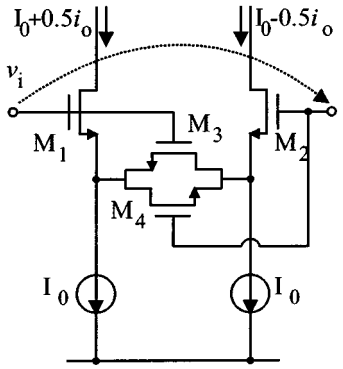

Fig. 2. MOS transconductor with source degeneration using MOS transistors.

gion and the channel length modulation effect will be neglected for simplicity. Therefore, the drain current is given by

$$I_D = \frac{\beta}{2}(V_{GS} - V_T)^2 \tag{1}$$

where β is the transconductance parameter and V_T is the threshold voltage of the MOS transistor.

Using (1) the simple differential MOS transconductor shown in Fig. 1(a) has a transfer characteristic given by

$$i_o = \sqrt{2\beta I_0}v_i\sqrt{1-\frac{\beta v_i^2}{8I_0}} = \sqrt{2\beta I_0}v_i\sqrt{1-\frac{v_i^2}{4(V_{GS}-V_T)^2}}. \tag{2}$$

Better linearity can be achieved for large effective gate-to-source voltages, $V_{GS_{\text{eff}}} = V_{GS} - V_T$. For low-voltage applications this constitutes a major drawback.

One of the simplest topologies to linearize the transfer characteristic of the MOS transconductor is the one with source degeneration using resistors and depicted in Fig. 1(b). The disadvantage of this configuration is the large resistor value needed to achieve a wide linear input range. Since in this case $G_m \approx 1/R$, the obtained transconductance is restricted to small values. Moreover, this technique eliminates the electronic tuning capability of the transconductance because its value is set by the degeneration resistor.

B. MOS Transconductors With Source Degeneration Using MOS Transistors

By replacing the degeneration resistors with two MOS transistors operating in the triode region, the circuit in Fig. 2 is obtained. Considering perfectly matched transistors M_1–M_2, M_3–M_4, and neglecting the body and channel length modulation effects, the transfer characteristic of this transconductor is given by

$$i_o = \frac{\sqrt{2\beta_1 I_0}}{a}\,v_i\sqrt{1-\frac{\beta_1 v_i^2}{a^2 I_0}} \tag{3}$$

where

$$a = 1 + \frac{\beta_1}{4\beta_3}. \tag{4}$$

Usually, the nonlinear term under the square root can be made much smaller than unity and improved linearity and larger input dynamic range can be obtained. However, increased linearity means smaller equivalent transconductance and reduced tuning capability. The circuit has bandwidth and noise performances comparable to the simple differential pair.

When the input voltage increases beyond a certain value

$$|v_i| > \sqrt{\frac{4I_0}{\beta_1}}\frac{a}{\sqrt{1-2a+2a^2}} \tag{5}$$

one of the two degeneration transistors enters in the saturation region (M_4 for $v_i > 0$, respectively M_3 for $v_i < 0$). The output differential current in this case is given by

$$i_o = \left(\frac{v_i\sqrt{\beta_1(4a-2)} + \sqrt{(8a-2)I_0 - \beta_1 v_i^2}}{4a-1}\right)^2. \tag{6}$$

In Fig. 3(a) the relative error of the transconductance $G_m(v_i) = di_o/dv_i$ derived from eqs. (3)–(6) is plotted for different values of parameter a. It can be easily seen and it was also shown in [1] that one can increase the input linear dynamic range by appropriately setting the value of parameter a (somewhere between 2.5 and 2.75). However, the nonlinearity error is up to 1% for $i_o/I_0 < 80\%$. In some filtering applications it is required to have better linearity in order to achieve a THD of -60 dB or less.

C. Adaptively Biased MOS Transconductors

Another topology to achieve high frequency linear MOS transconductors was reported in [2]. The idea is to use a tail current containing an input dependent quadratic component to cancel the nonlinear term in (2). Thus, if

$$I_0 = I_0' + \frac{\beta v_i^2}{8} \tag{7}$$

the transfer characteristic becomes linear

$$i_o = \sqrt{2\beta I_0'}v_i. \tag{8}$$

The required biasing current can be easily obtained using another two MOS transistors M_5–M_6 having identical transconductance coefficients as the ones in the differential pair M_1–M_2 and two unit-gain current mirrors M_7–M_8 and M_9–M_{10} as it is shown in Fig. 4. Additional circuitry is needed for generating the tuning voltage V_{BIAS}. The noise generated by the squaring circuitry does not appear at the output of the transconductor since it is like a common mode voltage at the sources of the differential

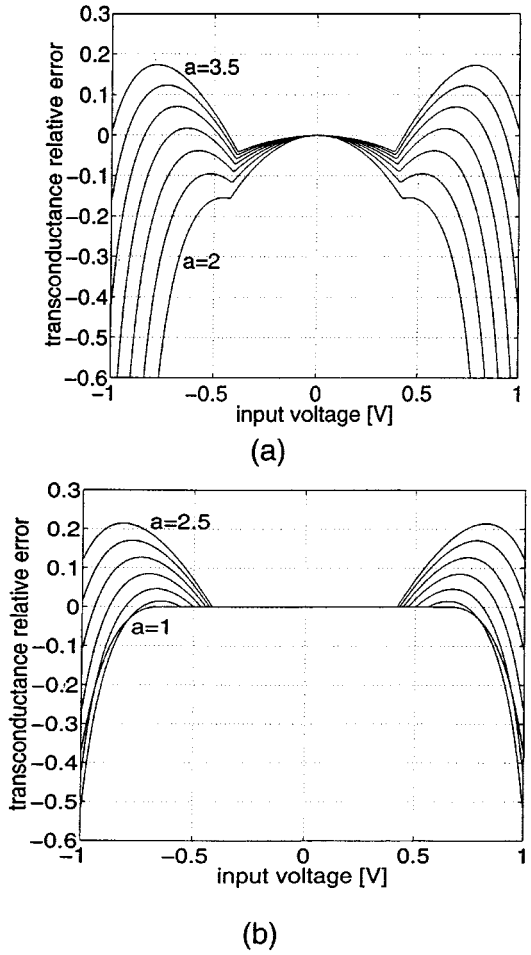

Fig. 3. Relative transconductance error for the MOS transconductors. (a) Using source degeneration with MOS transistors. (b) Using source degeneration with MOS transistors and adaptive biasing. Parameter a is varied with a step of 0.25.

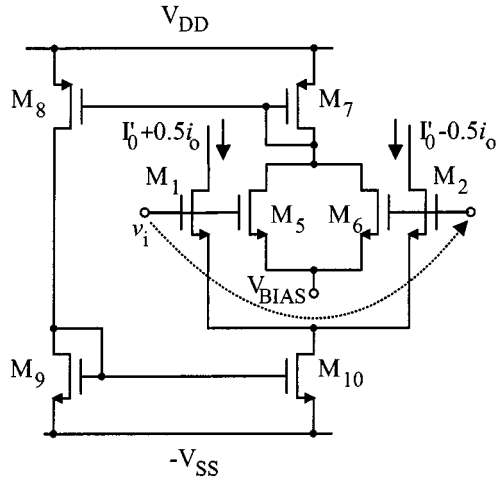

Fig. 4. Adaptively biased MOS transconductor.

pair. It was shown in [9] that due to the effect of mobility reduction, the size of the transistors in the squaring circuitry should be computed as a function of the voltage V_{BIAS} in order to obtain the best linearity. Therefore, tuning the circuit by means of V_{BIAS} will worsen the linearity. The class of input signals

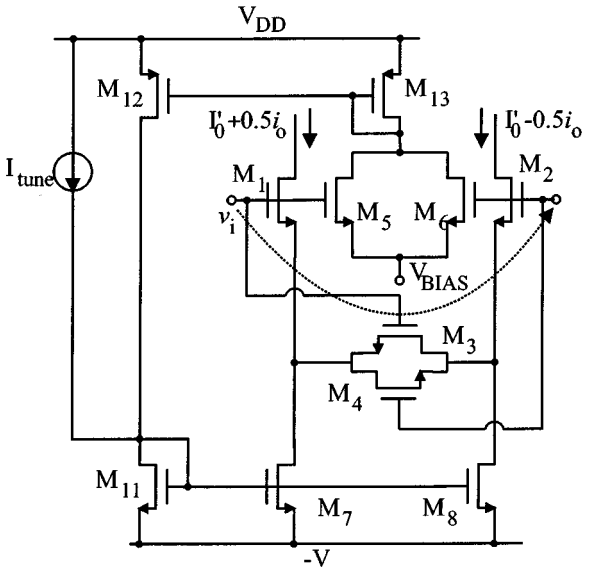

Fig. 5. Proposed linear MOS transconductor.

which can be processed is limited since the requirement of fully balanced signals is needed for the squaring circuit to function properly [9].

D. A Linear MOS Transconductor Using Source Degeneration and Adaptive Biasing

We propose another MOS transconductor that combines the two linearization approaches presented above. Starting from circuit in Fig. 2 and using adaptive biasing current sources, the circuit depicted in Fig. 5 is obtained. To transform the nonlinear transfer characteristic (3) into a linear one, the tail current I_0 should have the expression

$$I_0 = I_0' + \frac{\beta_1 v_i^2}{8a^2}. \tag{9}$$

The transfer characteristic becomes linear and is given by

$$i_o = \frac{\sqrt{2\beta_1 I_0'}}{a}\, v_i. \tag{10}$$

The adaptive bias current is

$$I_0 = I_{tune} + \beta_5 (V_{GS5} - V_T)^2 + \frac{\beta_5 v_i^2}{4} = I_0' + \frac{\beta_5 v_i^2}{4}. \tag{11}$$

Comparing (9) and (11), the transconductance coefficient of the squaring circuit should be

$$\beta_5 = \beta_6 = \frac{\beta_1}{2a^2}. \tag{12}$$

Since β_5 is smaller than β_1, the dc component of the current generated by the squaring circuitry is small compared to the necessary value required to bias the differential pair. Therefore, an additional current source I_{tune} is needed to tune the transconductor.

When the input voltage increases above the value

$$|v_i| > \frac{2a}{2a-1}\sqrt{\frac{2I_0'}{\beta_1}} \tag{13}$$

one of the transistors M_3, M_4 enters in the saturation region and the output differential current is given by

$$i_o = \left(\frac{v_i\sqrt{\beta_1(4a-2)} + \sqrt{(8a-2)I_0' - \left(\frac{2a-1}{2a}\right)^2 \beta_1 v_i^2}}{4a-1} \right)^2. \tag{14}$$

Fig. 3(b) shows the computed relative transconductance error for the circuit in Fig. 5, assuming quadratic MOS i–v characteristics (1). Imposing a certain maximum nonlinearity error, the value of parameter a can be computed. In practice, deviations from the quadratic MOS i–v characteristic due to mobility reduction and the body effect cause incomplete cancellation in (3). Therefore, the transconductance characteristic presents a certain curvature even for the case when both transistors M_3–M_4 are in the triode region. SPICE simulations using BSIM3v3 MOSFET models have shown that the best linearity can be achieved by setting the value of the parameter a between 1.5 and 1.75.

III. Simulation and Experimental Results

A. Comparison of Different Linearization Techniques

In order to compare the performance of different linearization techniques, numerous computer simulations have been run. To obtain a fair and accurate comparison, the circuits presented in Section II have been optimized to achieve the best linearity possible for a given transconductance value. SPICE simulated transconductance as a function of the input differential voltage is plotted in Fig. 6. From the detail shown in Fig. 6(b) it can be easily seen that the linearity achieved by the newly proposed configuration is better than all the other ones. The figure also included the results obtained in the case of a transconductor with resistive source degeneration and adaptive biasing, for comparison purposes.

The THD of the output differential current versus the amplitude of the input voltage for the three transistor-only linearized transconductors is depicted in Fig. 7. The topology in Fig. 4 achieves THD less than -57 dB for 1.6 V_{pp} input voltage, 10 dB better than the one without adaptive biasing and 27 dB better than the one using only adaptive biasing, for the same input range. For the same designed transconductance value, the novel proposed configuration is the second best as far as the power consumption and die area. It is surpassed only by the circuit in Fig. 4 for which the linearity is strongly dependent on the tuning voltage.

Fig. 8 illustrates the linearity performance of the three transistor-only transconductors when tuned for several transconductance values. The transconductor in Fig. 4 is tuned by changing V_{BIAS}, the one in Fig. 2 by changing the tail currents I_0, and the newly proposed one by changing I_{tune}. Our approach is again the best one.

Since the squaring circuitry used in adaptive biasing is properly functioning only for fully balanced inputs, the behavior of the MOS transconductors has been studied in the case of unbalanced input as well. Because the quadratic component of the

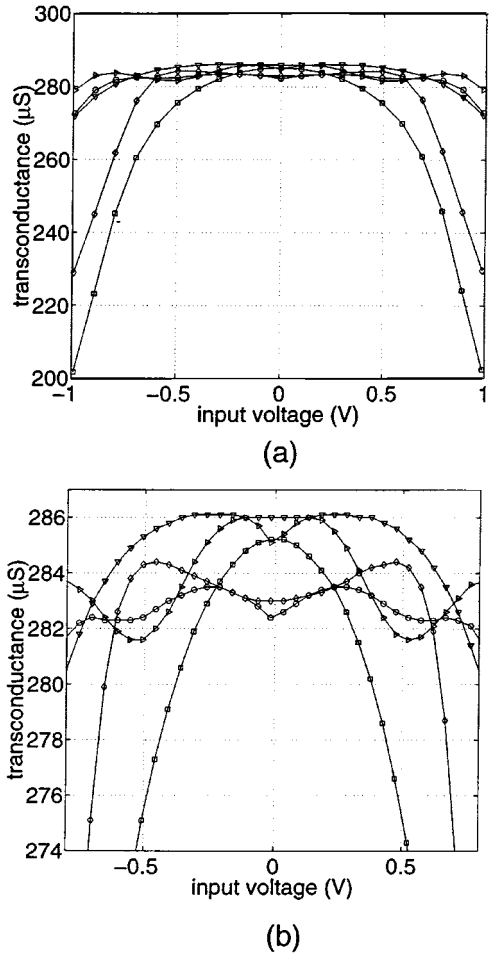

Fig. 6. Simulated transconductance for five linearization techniques. (a) Full plot. (b) Detail. (□) resistive source degeneration; (▽) resistive source degeneration with adaptive biasing; (▷) source degeneration using MOS transistors; (◇) adaptive biasing; (○) source degeneration using MOS transistors and adaptive biasing.

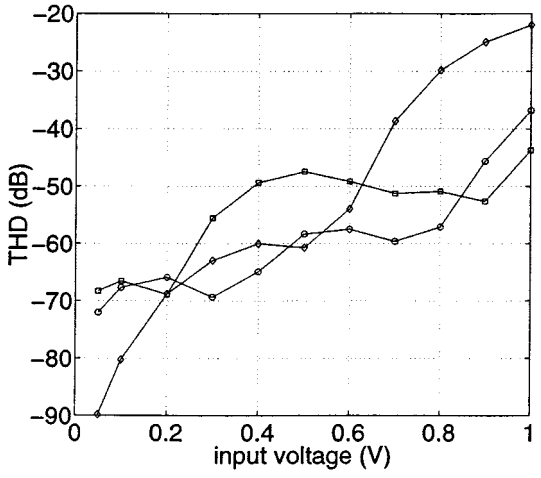

Fig. 7. Simulated THD at 1 kHz for the three resistor-free linearization techniques. (□) source degeneration using MOS transistors; (◇) adaptive biasing; (○) source degeneration using MOS transistors and adaptive biasing.

adaptive biasing current for the proposed circuit is smaller than the one needed for the configuration in Fig. 4 [see (7) and (9)], the linearity of the newly introduced transconductor degrades

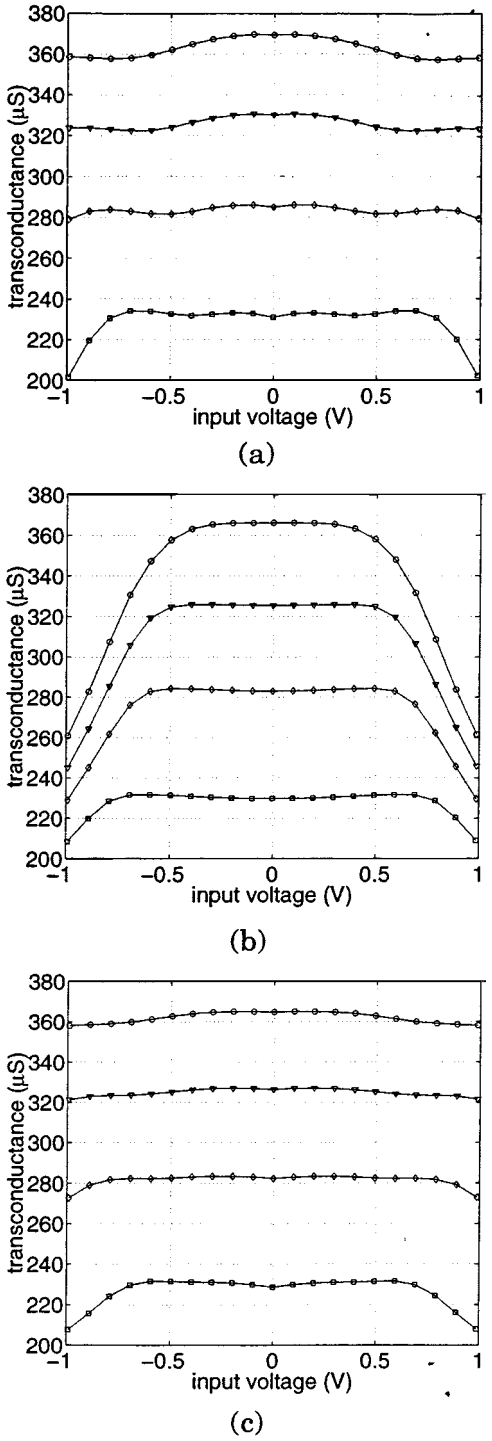

Fig. 8. Simulated transconductance of three linearized MOS transconductors under tuning. (a) Source degeneration using MOS transistors. (b) Adaptive biasing. (c) Source degeneration using MOS transistors and adaptive biasing.

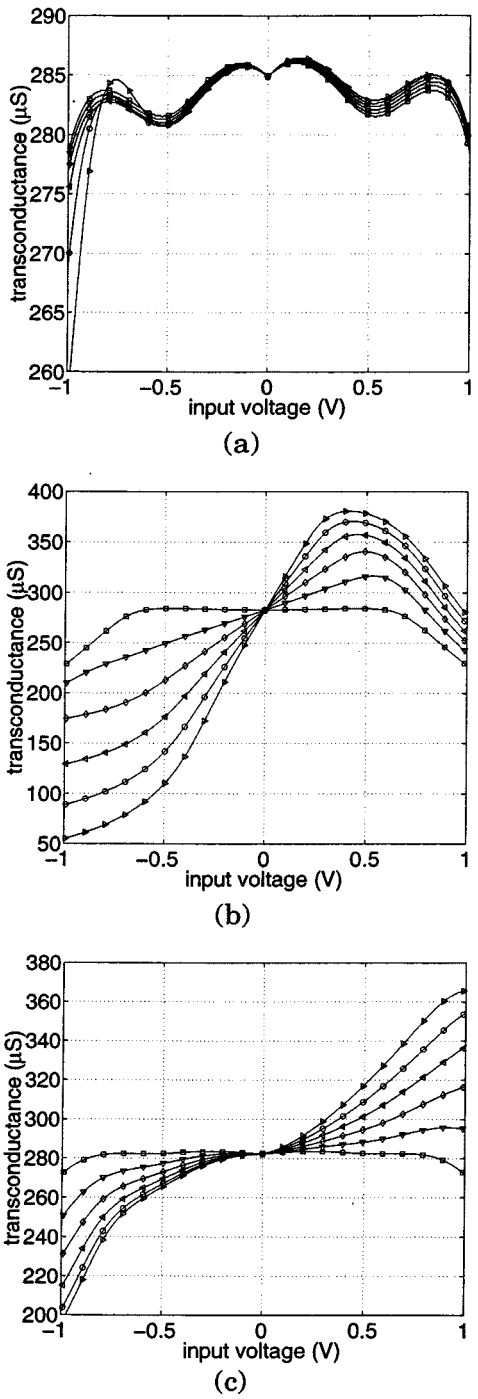

Fig. 9. Simulated transconductance for the three resistor-free linearization techniques in the case of unbalanced input. (a) Source degeneration using MOS transistors. (b) Adaptive biasing. (c) Source degeneration using MOS transistors and adaptive biasing. (□) fully balanced; (▽) 20% unbalanced; (◇) 40% unbalanced; (◁) 60% unbalanced; (○) 80% unbalanced; (▷) 100% unbalanced.

less for unbalanced inputs. The obtained simulation results are depicted in Fig. 9 and they confirm the expected behavior.

B. Experimental Results

The linear MOS transconductor has been fabricated using the 0.35 μm process from TSMC. The diagram of the entire circuit is shown in Fig. 10. The active load M_9–M_{10} is controlled by the common mode feedback circuitry for adjusting the output common mode voltage to the desired value V_{ocm}. Transistors M_{36}–M_{38} supply the voltage V_{BIAS} and M_{14} generates I_{tune}. Tuning can be achieved by means of the triode transistor M_{23}. The start-up circuitry needed for the biasing part has been omitted in Fig. 10.

The fabricated prototype has been designed for use in a continuous-time low-pass delta-sigma modulator. Very large area

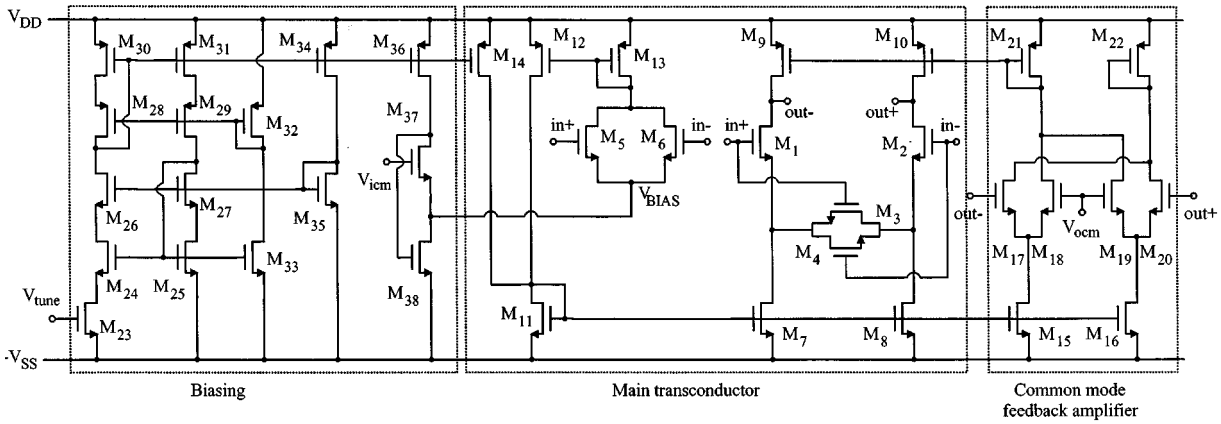

Fig. 10. Full circuit diagram of the fabricated transconductor.

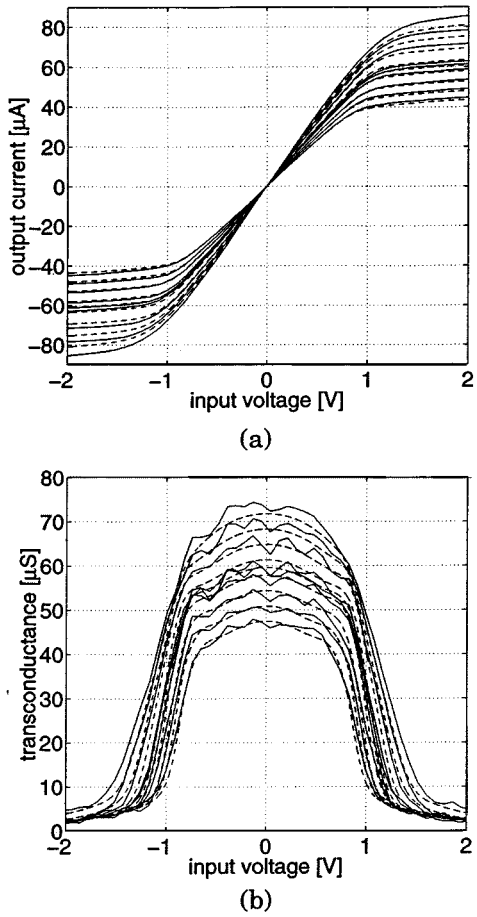

Fig. 11. Simulated (dotted lines) and measured (continuous lines) dc response. (a) i–v transfer characteristic. (b) Transconductance.

transistors are used in the output stage to minimize $1/f$ noise, with an active area of 0.47 mm^2 for the entire transconductor. A single supply voltage of 3.3 V has been used and the entire transconductor dissipates 1 mW for $G_m = 40\ \mu S$ and 5-MHz bandwidth. The relative low value of the transconductance is limited by the application, and reduces the input linear range compared to the optimal values obtained for the simulations in the previous section.

The simulated and measured dc characteristics are shown in Fig. 11. The transconductance plot has been obtained by differentiating the measured output i–v characteristic. The ripple is caused by the small number of points and finite precision of the measurement. The measured THD is approximately 6 to 10 dB larger than the simulated one. This is caused by the nonperfect matching of the transistors and, possibly, by the additional distortions introduced by the differential to single-ended conversion circuitry used in the measurement setup.

IV. Conclusion

An improved linear MOS transconductor, combining two linearization methods has been presented. The topology can achieve better linearity compared to other approaches and it can be used in implementing fully differential G$_m$-C continuous-time filters with severe linearity requirements. The proposed circuit has good tuning capability and it functions for both fully-balanced and unbalanced input signals, with some linearity depreciation in the latter case. In a practical implementation, the final linearity performance is set by the matching precision of the MOSFETs. The proposed circuit has been fabricated and experimental results agree with simulated linearity performance.

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