

# New General Immittance Converter JFET Voltage-Controlled Impedances and Their Applications to Controlled Biquads Synthesis

Adrian Leuciuc and Liviu Goraş

**Abstract**—Two new general immittance converter (GIC) JFET configurations for the realization of voltage-controlled impedances (VCI's) are proposed. Compared with previously reported structures, the circuits exhibit wide dynamic range and low distortion properties that are frequency independent, even for nonresistive VCI's. We consider the influence of op-amps frequency dependent gain and derive conditions for obtaining high  $Q$ -factor inductances and capacitances. We also present computed and experimental results for several voltage-controlled GIC-type biquads that are built based on the proposed circuits.

**Index Terms**—Active filters, active impedance simulation.

## I. INTRODUCTION

Several op-amp JFET structures for the realization of positive/negative voltage-controlled impedances (VCI's) have been previously reported [1]–[5]. All these configurations use the technique introduced in [1] by Nay and Budak. The nonlinear equation describing the JFET drain current  $I_D$  in the nonsaturated region is

$$I_D = \frac{I_{DSS}}{V_P^2} [2V_{DS}(V_{GS} - V_P) - V_{DS}^2] \quad (1)$$

where  $I_{DSS}$  is the saturation drain current and  $V_P$  is the threshold voltage. If the JFET gate-to-source voltage  $V_{GS}$  satisfies

$$V_{GS} = \frac{V_{DS} + V_C}{2} \quad (2)$$

where  $V_{DS}$  is the drain-to-source voltage and  $V_C$  is a control voltage, then the drain current  $I_D$  becomes linear in  $V_{DS}$  and

$$I_D = \frac{I_{DSS}}{V_P^2} (V_C - 2V_P)V_{DS}. \quad (3)$$

Equation (3) is valid only for small values of  $V_{DS}$ , and the extension of the linear range has been achieved by reducing the drain-to-source voltage of the JFET to a fraction  $a \ll 1$  of the input voltage  $V$  to keep the JFET in the nonsaturated region. Hence,

$$V_{DS} = aV. \quad (4)$$

Even though these realizations manifest good linearity and wide dynamic range, they have several disadvantages. The structures proposed in [1], [2], and [5] can be used to realize resistive impedances only, while the structure introduced in [3] does not allow the realization of purely inductive impedances. Furthermore, since for the realization [3] the parameter  $a$  (4) depends on the drain-to-source JFET resistance, the linear dynamic range is drastically reduced, and the distortions increase for large values of the realized impedance. By using a supplementary op-amp and several resistors, the circuits proposed in [4] can realize positive and negative impedances, including inductances. Furthermore, the value of  $a$  is independent of JFET parameters and is determined by the ratio of two impedances. However, the circuits possess conditional stability and linear range

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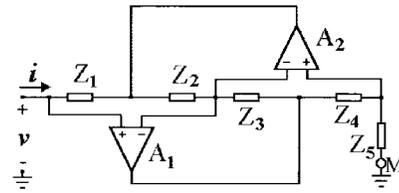


Fig. 1. Antoniou's general immittance converter (GIC).

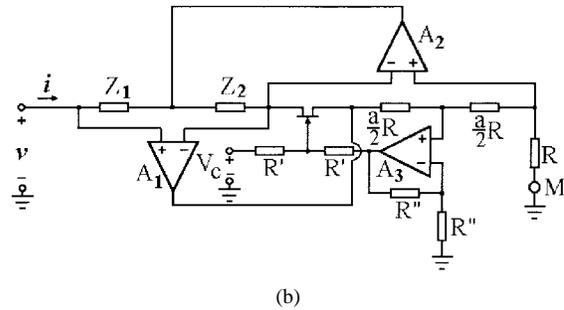
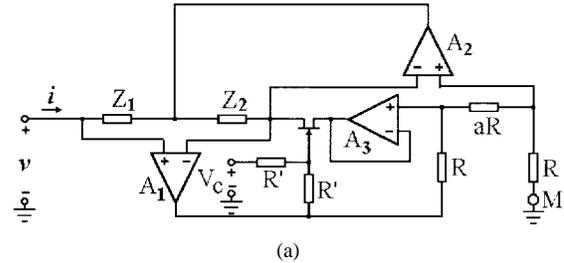


Fig. 2. GIC-JFET proposed structures for the realization of VCI's.

that is frequency dependent for nonresistive VCI's. In this brief we present two new structures that eliminate these inconveniences.

## II. PROPOSED CONFIGURATIONS

The new configurations proposed in this paper use the well-known Antoniou's general immittance converter (GIC) structure [6], [7] shown in Fig. 1 that has input impedance

$$Z_{in} = \frac{Z_1 Z_3 Z_5}{Z_2 Z_4}. \quad (5)$$

Basically, the control of the impedance value  $Z_{in}$  can be achieved by replacing one of the impedances  $Z_i$ ,  $i = 1, \dots, 5$ , with a JFET operating in the nonsaturated region. To fulfill the conditions (2) and (4), a supplementary op-amp is embedded into the GIC structure, the impedances  $Z_4$  and  $Z_5$  are replaced by two resistances  $R_4 = aR$  and  $R_5 = R$ , and the impedance  $Z_3$  is replaced by the JFET drain source as shown in Fig. 2. Under the hypothesis of ideal op-amps and operation of JFET in the nonsaturated region (neglecting the gate current), a straightforward analysis yields the following expression for the realized impedance:

$$Z_{in} = \frac{Z_1 R_{JFET}}{a Z_2} \quad (6)$$

where  $R_{JFET} = \frac{V_P^2}{I_{DSS}(V_C - 2V_P)}$  is the drain-to-source resistance of the JFET.

The drain-to-source voltage is given by (4) with  $a = R_4/R_5$ . It is independent of  $Z_1$ ,  $Z_2$ , and of the transistor parameters. Compared

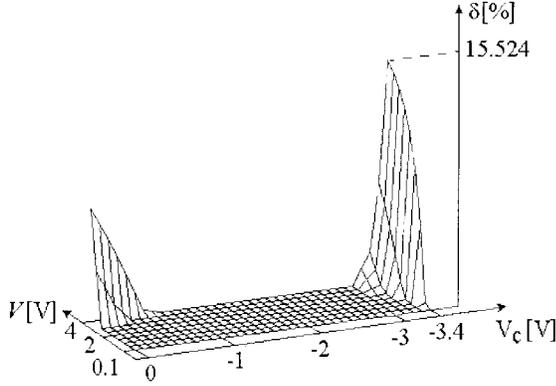


Fig. 3. Dependence of the total harmonic distortion coefficient on the amplitude of the input voltage  $V$  and on the magnitude of the control voltage  $V_C$ . The plot corresponds to the voltage-controlled resistance realized with the circuit shown in Fig. 2(a). Parameters:  $R_1 = 1 \text{ k}\Omega$ ,  $R_2 = 10 \text{ k}\Omega$ ,  $R = 15 \text{ k}\Omega$ , and  $R' = 100 \text{ k}\Omega$ . The first nine harmonics have been taken into account.

with the positive VCI configuration proposed in [4], which may also realize resistive, capacitive, and inductive impedances, the circuits shown in Fig. 2 have the following advantages.

- The drain-to-source voltage is independent of  $Z_1$  and  $Z_2$ . Thus, the linear dynamic range is frequency independent even for nonresistive VCI's (main advantage).
- Even though they also contain three op-amps, these circuits are simpler because they require only five [circuit shown in Fig. 2(a)] or seven [circuit shown in Fig. 2(b)] resistors instead of nine.

### III. INFLUENCE OF THE FREQUENCY DEPENDENT FINITE GAINS OF OP-AMPS

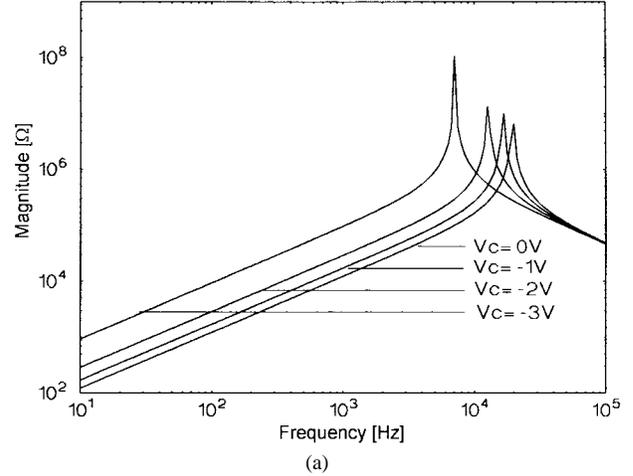
A nullator-norator structure equivalent to the circuit shown in Fig. 2(a) has been analyzed in [8] and [9]. It has been shown there that the frequency range drastically decreases for high- $Q$  inductances. The circuit shown in Fig. 2(a) was obtained from [8] and [9] by op-amp relocation technique [10], [11] and has a superior frequency range.

Considering finite gain op-amps, the input current  $i$  and voltage  $v$  have nonlinear dependence due to the inaccurate realization of (2). However, if the quantity  $(V_C - 2V_P)$  is not too small, this dependence becomes linear and leads to the expression for the realized impedance (7), shown at the bottom of the page. For  $\omega \ll \omega_{tk}$ , where  $\omega_{tk}$  is the gain bandwidth product of the  $k$ th op-amp, the one pole transfer function of the  $k$ th op-amp can be approximated with

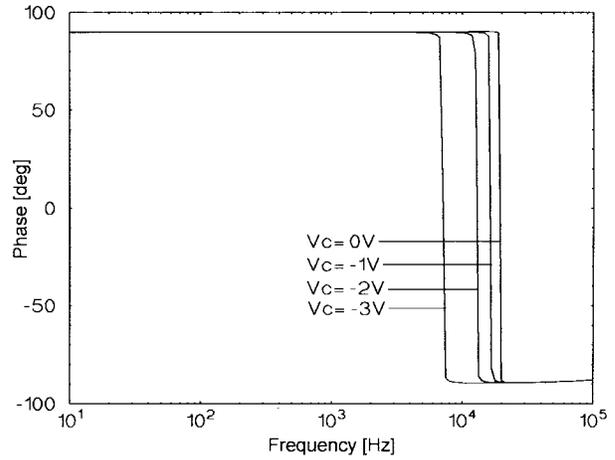
$$A_k \approx \frac{\omega_{tk}}{s}. \quad (8)$$

From (7) and (8) it is easy to find that for identical op-amps, the impedance  $Z_{in}$  is positive real if either  $Z_1$  and  $Z_2$  are resistive or if one of them is capacitive. Thus, in these cases, the circuit is both open-circuit and short-circuit stable.

Since in controlled biquad synthesis we shall use mainly voltage-controlled inductances, we consider the case  $Z_1 = R_1$  and  $Y_2 = sC_2$ .



(a)



(b)

Fig. 4. Simulated (a) magnitude and (b) phase of  $Z_{in}(j\omega)$  for the circuit shown in Fig. 2(a), the inductive case. Parameters:  $R_1 = 10 \text{ k}\Omega$ ,  $C_2 = 100 \text{ nF}$ ,  $R = 15 \text{ k}\Omega$ ,  $R' = 100 \text{ k}\Omega$ ,  $C_{comp1} = C_{comp3} = 30 \text{ pF}$ , and  $C_{comp2} = 36 \text{ pF}$ .

Neglecting second-order terms in  $\omega/\omega_{tk}$ , we obtained the relation for the input impedance valid for  $\omega \ll \omega_{tk}$

$$Z_{in} = j\omega C_2 R_1 R_3 \times \frac{1 + \frac{1+a}{\omega_{t2} C_2 R_3} + j\omega \left[ \frac{1}{\omega_{t3}} + \frac{2+a}{\omega_{t1}} + \frac{2+a}{\omega_{t1} \omega_{t2} C_2 R_3} \right]}{a + j\omega \left[ \frac{1+a}{\omega_{t2}} - \frac{1}{\omega_{t3}} \right]}. \quad (9)$$

High- $Q$  voltage-controlled inductance can be obtained if

$$\frac{1+a}{\omega_{t3}} + \frac{a(2+a)}{\omega_{t1}} - \frac{1+a}{\omega_{t2}} = 0, \quad C_2 R_3 \gg \frac{1}{\omega_{tk}}. \quad (10)$$

For  $\omega_{t1} = \omega_{t3} = \omega_t$ , the first condition in (10) becomes

$$\omega_{t2} = \frac{a+1}{a^2+3a+1} \omega_t. \quad (11)$$

If  $a \rightarrow 0$ , then  $\omega_{t2} \rightarrow \omega_t$ . If, for example,  $a = 0.1$ , then  $\omega_{t2} = 0.84\omega_t$ .

$$Z_{in} = Z_1 \frac{R_{JFET} \left[ 1 + \frac{2+a}{A_1} \left( 1 + \frac{1}{A_2} \right) \right] \left( 1 + \frac{1}{A_3} \right) + Z_2 \left[ \frac{2+a}{A_1 A_2} \left( 1 + \frac{1}{A_3} \right) + \frac{1+a}{A_2} \right]}{R_{JFET} \frac{2+a}{A_1} \left( 1 + \frac{1}{A_2} \right) \left( 1 + \frac{1}{A_3} \right) + Z_2 \left[ a + \frac{2+a}{A_1 A_2} \left( 1 + \frac{1}{A_3} \right) + \frac{1+a}{A_2} - \frac{1}{A_3} \right]} \quad (7)$$

TABLE I

Filter type	Schematic	Transfer function	Observations
Band-pass		$H(s) = \frac{k \frac{s}{R_0 C_0}}{s^2 + \frac{s}{R_0 C_0} + \frac{a}{C_0 C_2 R_1 R_{JFET}}}$	Valid for both structures of Fig. 2. k=(2+a) for the circuit of Fig. 2(a); k=(1+a) for the circuit of Fig. 2(b).
High-pass		$H(s) = \frac{ks^2}{s^2 + \frac{s}{R_0 C_0} + \frac{a}{C_0 C_2 R_1 R_{JFET}}}$	Valid for both structures of Fig. 2. k has the same values as above.
Notch		$H(s) = \frac{s^2 + \frac{a}{C_2 C_0 R_1 R_{JFET}}}{s^2 + s \frac{(1+a)}{a R_0 C_0} + \frac{a}{C_2 C_0 R_1 R_{JFET}}}$	Valid only for the structure of Fig. 2(b).
Low-pass		$H(s) = \frac{\frac{a^2}{(a+1)C_2 C_0 R_1 R_{JFET}}}{s^2 + s \frac{1}{R_0 C_0} + \frac{a^2}{(a+1)C_2 C_0 R_1 R_{JFET}}}$	Valid only for the structure of Fig. 2(b).

For the voltage-controlled capacitance realization, condition (10) should also be satisfied. Relation (11) can be obtained by compensating the op-amps with appropriate capacitors in order to satisfy the specified ratio between the gain-bandwidth products.

The circuit shown in Fig. 2(b) is also derived from the GIC structure where the resistive impedance  $Z_4$  has been split into two parts. A supplementary op-amp  $A_3$  and two resistors  $R''$  have been added to fulfill conditions (2) and (4). The condition for obtaining high- $Q$  voltage-controlled inductances ( $Z_1 = R_1$ ,  $Y_2 = sC_2$ ) is  $\omega_{t1} = a\omega_{t2} \ll \omega_{t2}$ , and it restricts the frequency range. Even though this circuit has two extra resistors compared with the circuit shown in Fig. 2(a), it has an important advantage that will be pointed out in the next section.

#### IV. VOLTAGE-CONTROLLED BIQUADS

It is well known that the general transfer function of a biquad is given by

$$H(s) = \frac{P(s)}{s^2 + B_p s + \omega_n^2} \quad (12)$$

where  $P(s)$  is a polynomial of second order in  $s$ ,  $B_p$  is the angular pole bandwidth, and  $\omega_n$  is the undamped natural angular frequency. We have studied the performances of four types of voltage-controlled biquads derived from the Antoniou's GIC structure (with  $Z_1 = R_1$ ,  $Y_2 = sC_2$ ) and they are the band-pass, high-pass, notch, and low-pass. The corresponding configurations are given in Table I,  $\omega_n$  being the only parameter affected by the control voltage in all cases. The

output signal is the output voltage of op-amp  $A_1$ . Unfortunately, the notch and the low-pass biquads cannot be realized using the structure shown in Fig. 2(a) because the relation (2) is no more valid when the node  $M$  is not grounded. Thus, the advantage of the circuit shown in Fig. 2(b), which can be viewed as a voltage-controlled GIC, is its versatility.

We also examined the influence of the op-amps limited bandwidth on the deviations in natural frequency and  $Q$ -factor for the biquads shown in Table I. The results showed that this influence can be reduced if the following relations are fulfilled:

$$C_2 R_{JFET} \omega_{tk} \gg 1 \quad C_0 R_0 \omega_{tk} \gg 1 \quad C_0 R_1 \omega_{tk} \gg 1, \quad \text{for } k = 1, 2, 3. \quad (13)$$

For the band-pass and high-pass biquads based on the structure shown in Fig. 2(a), the deviations of  $Q$ -factor can be further diminished if  $\omega_{t2} = (a+1)\omega_{t3}$ . Compared with operational transconductance amplifiers (OTA) based realizations of voltage-controlled biquads [12], for example, except for high-frequency performances, the proposed circuits are more flexible because various types of filtering functions can be obtained with slight modifications.

#### V. RESULTS

The SPICE computer simulations and the experiments were carried out using 748-type op-amps (which allow bandwidth control by using a compensating capacitor), a BF245-type JFET ( $I_{DSS} = 4.5$  mA,  $V_P = -1.72$  V),  $a = 0.1$ , and supply voltages of  $\pm 15$  V.

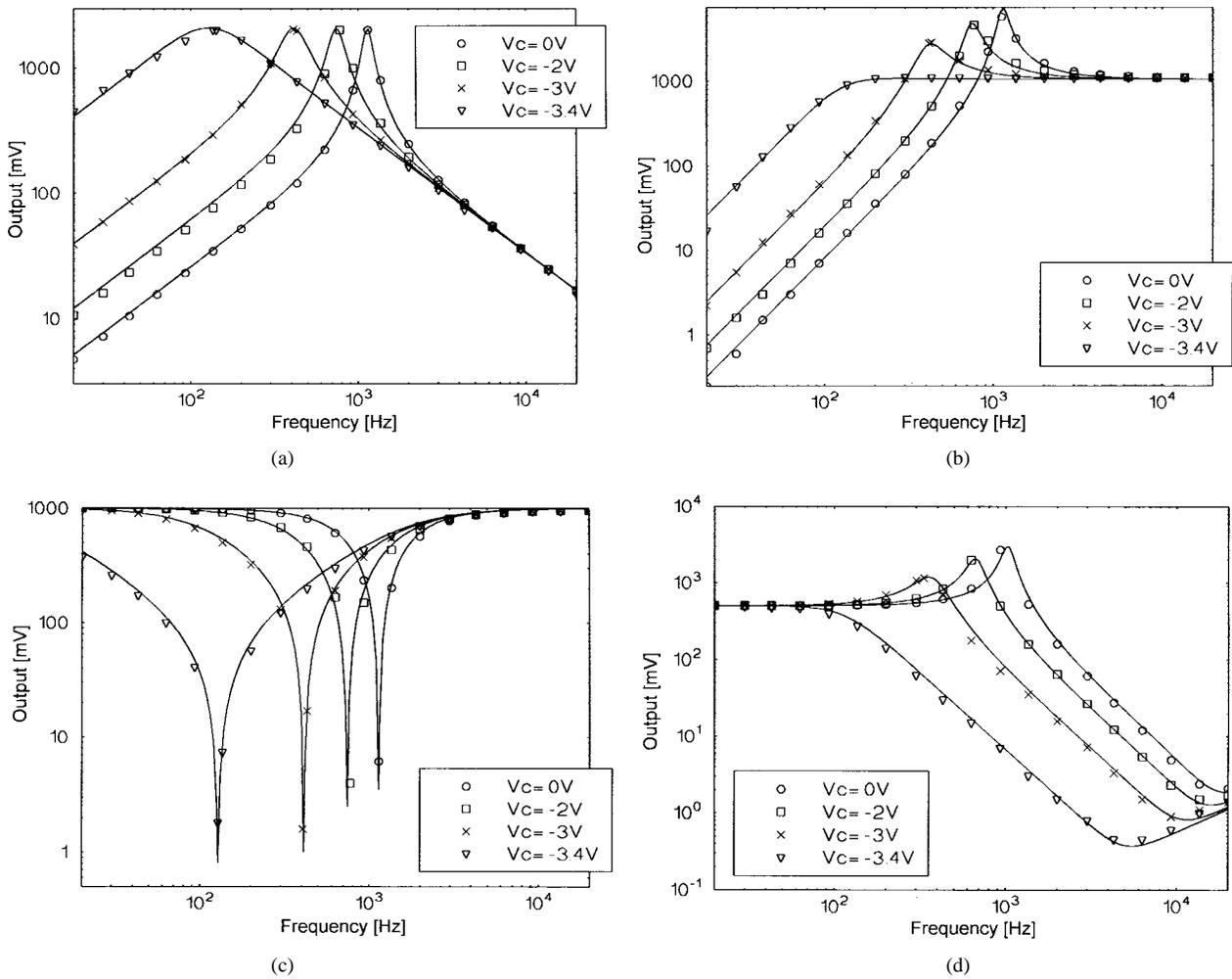


Fig. 5. Experimental (represented with marked points) and simulated (represented with lines) magnitude characteristics of the four types of voltage-controlled biquads shown in Table I: (a) band-pass (input =  $1 V_{\text{rms}}$ ,  $R_1 = 10 \text{ k}\Omega$ ,  $C_2 = 100 \text{ nF}$ ,  $R = 15 \text{ k}\Omega$ ,  $R' = 100 \text{ k}\Omega$ ,  $R_0 = 100 \text{ k}\Omega$ , and  $C_0 = 10 \text{ nF}$ ); (b) high-pass (input =  $0.5 V_{\text{rms}}$  and the same values as in the band-pass case); (c) notch (input =  $1 V_{\text{rms}}$ ,  $R_1 = 10 \text{ k}\Omega$ ,  $C_2 = 100 \text{ nF}$ ,  $R = 30 \text{ k}\Omega$ ,  $R' = 100 \text{ k}\Omega$ ,  $R_0 = 100 \text{ k}\Omega$ , and  $C_0 = 10 \text{ nF}$ ); and (d) low-pass (input =  $0.5 V_{\text{rms}}$ ,  $R_1 = 1 \text{ k}\Omega$ ,  $C_2 = 100 \text{ nF}$ ,  $R = 30 \text{ k}\Omega$ ,  $R' = 100 \text{ k}\Omega$ ,  $R_0 = 100 \text{ k}\Omega$ , and  $C_0 = 10 \text{ nF}$ ).

The computed harmonic distortion coefficient  $\delta$  versus the amplitude of the input voltage  $V$  and the value of the control voltage  $V_C$  for the voltage-controlled resistance obtained with the structure shown in Fig. 2(a) is shown in Fig. 3. As it can be easily observed,  $\delta$  increases both with the amplitude of the input voltage and the magnitude of  $V_C$ . An increase in the harmonic distortion coefficient appears even for small values of  $|V_C|$ . This is due to the nonlinear behavior of op-amp  $A_2$ , which saturates for large amplitudes of the input voltage. When the saturation of op-amps does not occur and for control voltages in the range  $-3 \text{ V} \leq V_C \leq 0$ , the harmonic distortion coefficient is smaller than 0.06%.

SPICE simulated magnitude and phase of the input impedance of the circuit shown in Fig. 2(a) (with  $Z_1 = R_1$  and  $Y_2 = sC_2$ ) are shown in Fig. 4. The op-amps  $A_1$  and  $A_3$  were compensated with 30 pF capacitors, while  $A_2$  was compensated with 36 pF to satisfy (11) and to obtain a high- $Q$  inductance. In the worst case ( $V_C = -3 \text{ V}$ ) the phase error is under one degree up to 6 kHz.

The experimental and simulated magnitude characteristics for the four types of voltage-controlled biquads of Table I are shown in Fig. 5. The band-pass and the high-pass filters were realized with the circuit shown in Fig. 2(a), while the notch and low-pass filters were realized with the circuit shown in Fig. 2(b). As it can be seen from Fig. 5, varying the control voltage from  $-3.4 \text{ V}$  to  $0 \text{ V}$ , the parameter

$\omega_n$  can be modified over a decade. A wider range could be achieved using JFET's with greater threshold voltage  $V_P$ .

## VI. CONCLUDING REMARKS

The performances of the circuits proposed in this paper are superior compared to the previous reported structures of op-amp JFET-based VCI's. These new configurations that can find applications in self-tuning filters, voltage-controlled oscillators, and nonlinear synthesis [13], exhibit very good linearity, wide dynamic range, low distortion properties, and unconditional stability.

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