Challenges and limits for very low energy computation

Francis Balestra
Sinano Institute, IMEP-Minatec (CNRS-Grenoble INP, UJF), France

The historic trend in micro/nano-electronics over the past 40 years has been to increase both speed and density by scaling down the electronic devices, together with reduced energy dissipation per binary transition. Today, we are facing dramatic challenges due to energy consumption (static and dynamic) and heat removal, inducing fundamental tradeoffs for the future ICs. Research into the ultimate reduction of computation dissipation is needed for the development of future high-performance tera-scale integration and autonomous (nano)systems. This paper addresses the main challenges, limits and possible solutions to strongly reducing the energy per binary switching. Several paths are possible: adiabatic logic using a slow clock, which will not be addressed here because it cannot be used for high-performance computing, logic stochastic resonance, or conventional logic with a reduction in the stored energy, therefore a decrease of device capacitance C (device integration) or applied bias V, which seems to be the most promising for future ICs.

The reduction of the stored energy in conventional logic can be done with a strong reduction in V using new physics and/or devices with sub-60mV/dec subthreshold swing S, which is the limit of MOSFETs at 300K. The following fundamental approaches have been suggested: energy filtering (tunnel FET, in MOS, nanowire (NW), CNT or graphene, using band-to-band tunnelling to filter the electron energy distribution, NW FETs with superlattice (*e.g.* InGaAs/InAlAs heterostructure) in the source, internal voltage step-up (ferroelectric gate FET, inducing a negative capacitance to amplify the change in channel potential induced by the gate), NEMS devices, or impact ionization MOS devices.

We will focus here on the best ones for ULSI, TFETs, using gate-controlled *pin* structures with carriers tunnelling through rather than diffusing over a barrier. The most interesting structures, proposed using experiments or numerical simulations with the aim of reducing the effective mass, the bandgap and/or the tunnelling length for increasing I_{ON} and reducing S for several decades of current, are the following: i) bandgap reduction using Ge or III-V channel materials (operation down to 0.2 V) (simul) [1], ii) InAs TFETs (SG, DG, GAA NW) with small bandgap and electron-hole effective mass, S down to 20 mV/dec for 2 nm nanowires or UTB double-gate TFETs (simul) [2], iii) uniaxial and biaxial strained InAs nanowire TFET with S down to 22 mV/dec and large I_{ON}/small switching delay (simul) [3], iv) HTFET using InGaAs with thin gate oxide, high source doping leading to sub-60 mV/dec (exp) [4], v) CNT tunnel FET with S = 40 mV/dec (exp) [5], vi) feedback TFET with gate-controlled injection barrier leading to very small S (exp) [6], vii) thin and double-gate SOI TFET with high-κ dielectrics, or SGOI, or GOI for higher I_{ON} (exp) [7, 8].

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