Hybrid CMOS/nanoelectronic circuits

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I propose to review the recent intensive work on several species of hybrid semiconductor/ nanodevice circuits – see, e.g., Refs. 1–3 for recent (mostly incomplete) reviews of the field. The idea behind all these suggestions is to combine the advantages of CMOS technology (including its high functionality, reliability, and flexibility) with extremely high potential density of simple nanodevices (at affordable cost of their "bottom-up" fabrication). Most of the hybrid circuit concepts are based on using nanowire crossbars with two-terminal nanodevices formed at each crosspoint.

Small (e.g., 34×34) crossbars of this type have been already demonstrated with nanowire half-pitch as small as 17 nm, and crosspoint device yield above 90%, and substantial improvement of all these parameters seems imminent. As a result, the focus of the conceptual work (and most controversy) has moved to the best ways of providing an efficient interface between the crossbar nanowires and the CMOS subsystem with much cruder design rules. For example, in our "CMOL" concept the interface is provided by vertical pins (with CMOS-scale pitch but nanometer-scale tips) which are distributed all over the circuit area. Somewhat counter-intuitively, a topological trick within this approach allows individual addressing of each nanodevice without nanoscale alignment of the crossbar and CMOS subsystems.

Several detailed studies have shown that hybrid CMOS/nanodevice circuits may provide unparalleled performance (at acceptable power dissipation), together with high defect tolerance (necessary when dealing with molecular-scale nanodevices) in at least thee application areas.

(i) *Memories.* Calculations show that a synergy of array reconfiguration with advanced error correction code techniques may enable memory chips with terabit-scale integration at sub-100-ns access time, with defect tolerance above 8%.

(ii) *FPGA-type reconfigurable logic circuits* may provide an least two orders of magnitude advantage over purely CMOS FPGAs (in the logic-area metric) at ITRS-specified power consumption and even higher (~20%) defect tolerance.

(iii) *Mixed-signal neuromorphic networks* ("CrossNets") based on hybrid circuits may be trained to perform all the basic function demonstrated earlier with software-implemented neural networks, despite the hardware-imposed restrictions. This fact is very significant taking into account that CrossNets may reach areal densities exceeding that of the human cerebral cortex, while operating at much higher speed, again at manageable power.

On the basis of these studies, I will argue that hybrid CMOS/nanoelectronic circuits may be the most straightforward (and perhaps the only) way to extend the Moore's Law well beyond the 10-nm frontier.

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2. P. Kuekes, G. Snider, and R. S. Williams, "Crossbar nanocomputers", *Sci. Amer*. **71**, 72 (Nov. 2005).
3. A. DeHon and K. Likharev, "Hybrid CMOS/nanoelectronic digital circuits: Devices, architectures, and design automation", *Proc. ICCAD-2005* (IEEE Press, Piscataway, NJ, 2005), pp. 375-382.