Future of nano CMOS and Its Manufacturing

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Recently, CMOS downsizing has been accelerated very aggressively both in production and at the research level, and even transistor operation of a 5 nm gate length CMOS was reported in a conference. However, many serious problems are expected for implementing small-geometry MOSFETs into large scale integrated circuits even for 45 nm technology node, and it is questionable whether we can successfully introduce sub-10 nm CMOS LSIs into market for many reasons, ranging from insufficient current drive to huge manufacturing costs. In this talk, technology and manufacturing issues for future CMOS scaling towards its limits are described. In order to solve the problems, the introduction of quite new technologies, such as new materials, processes, and structures are inevitable. Some of those efforts made in my laboratory are presented. They are high-κ dielectrics for gate insulators and plasma doping for ultra-shallow source and drain junctions. Furthermore, solutions and problems of the manufacturing cost increases will be discussed. Finally, the outlook for the post-scaling era will be predicted.