Ultimate VLSI clocking using passive serial distribution

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Despite the impressive transistor speeds of scaled VLSI technologies, clocking large chips such as microprocessors, FPGAs and ASICs at multi-GHz frequencies suffers from severe limitations. The main culprit is the well trusted but dated active tree clocking method, used in virtually all VLSI applications. Typically, a central PLL-synthesized clock signal is distributed to local areas through a very complex tree network including thousands of branches, amplifiers, buffers, phase adjustment circuits, *etc*. Maintaining low skew and low jitter with such "brute force" active clocking systems is extremely challenging and requires substantial power dissipation even at low GHz speeds. Noise leakage from adjacent digital blocks, power supply lines, *etc*. and absolute skew uniformity over all chip areas are particularly difficult to control. Clearly, there is an urgent need to develop a totally different and scalable solution to the VLSI clocking problem, a topic of worldwide research activities.

We introduce a new general principle for VLSI clocking using passive serial distribution. This approach is capable of very high operating speed, minimum jitter, and minimum power dissipation. We assume the availability of on-chip transmission lines. These can be either electrical lines built with standard CMOS metal levels or on-chip optical wave guides fabricated through additional processing steps. In the latter case, optical detectors are also necessary. The proposed architecture is a simple serial connection passing through all local clocking regions. For electrical lines with nonnegligible loss, a two-tier network would cover the largest chips in existence without excessive individual line lengths.

As the passive propagation of signals on transmission lines is insensitive to circuit noise, power supply voltage variations, *etc.*, the clock signals are distributed easily and accurately to any local area on the chip. However, for serial distribution very large skews accumulate quickly. The novelty of our approach consists of a simple signaling method allowing efficient and precise skew removal at any arbitrary clock drop-point along the transmission line. This open-loop synchronization technique is naturally insensitive to nonideal effects, such as ohmic losses, transmission line termination errors, and amplitude noise. We will discuss this signaling scheme and the supporting circuits, which are straightforward and easy to design. In addition, we will show simulation results using complex transmission line models and standard production CMOS transistor models.

In addition to frequency scalability and superior jitter/skew performance, our method promises a major simplification in the VLSI design methodology. While in the conventional case, the architecture, size, and physical position of the logic blocks are in close functional relationship with the clocking tree, this complicated interdependence is almost totally eliminated in our approach. The decoupling between the clocking system and its clocked "clients" brings a major simplification in the design methodology, transforming the clocking system design from a black art into a standard platform technology, a future CAD tool will implement automatically.