NANOELECTRONIC TECHNOLOGY: In Search of the Ultimate Device Structures

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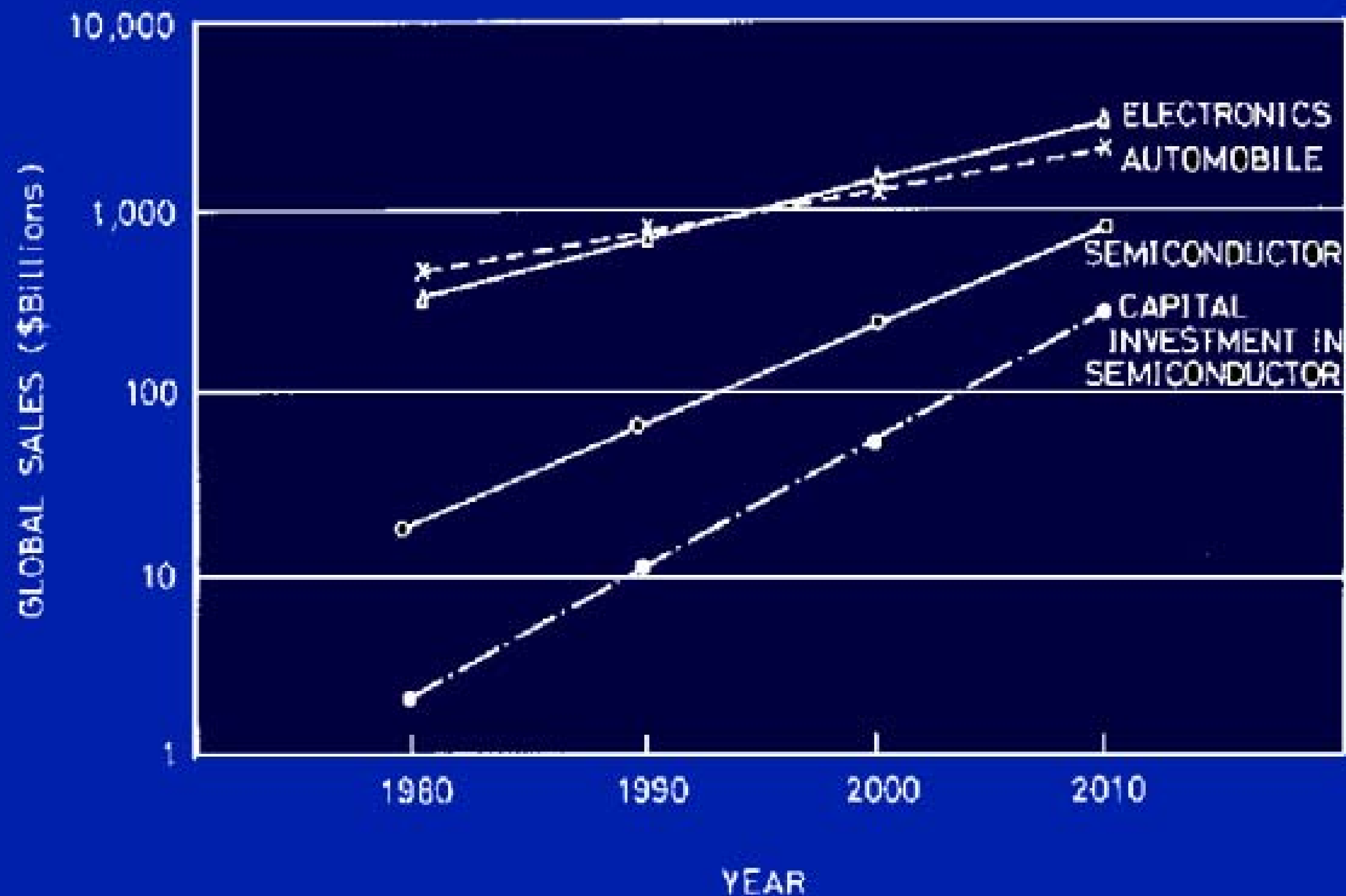
OUTLINE

- INTRODUCTION
- EVOLUTION OF MOSFET STRUCTURES
- MAJOR ISSUES OF DEVICE SCALING
- NANOTECHNOLOGY OPTIONS AND ULTIMATE DEVICE
- CONCLUSION

SEMICONDUCTOR INDUSTRY: A KEY INDUSTRY FOR 21ST CENTURY

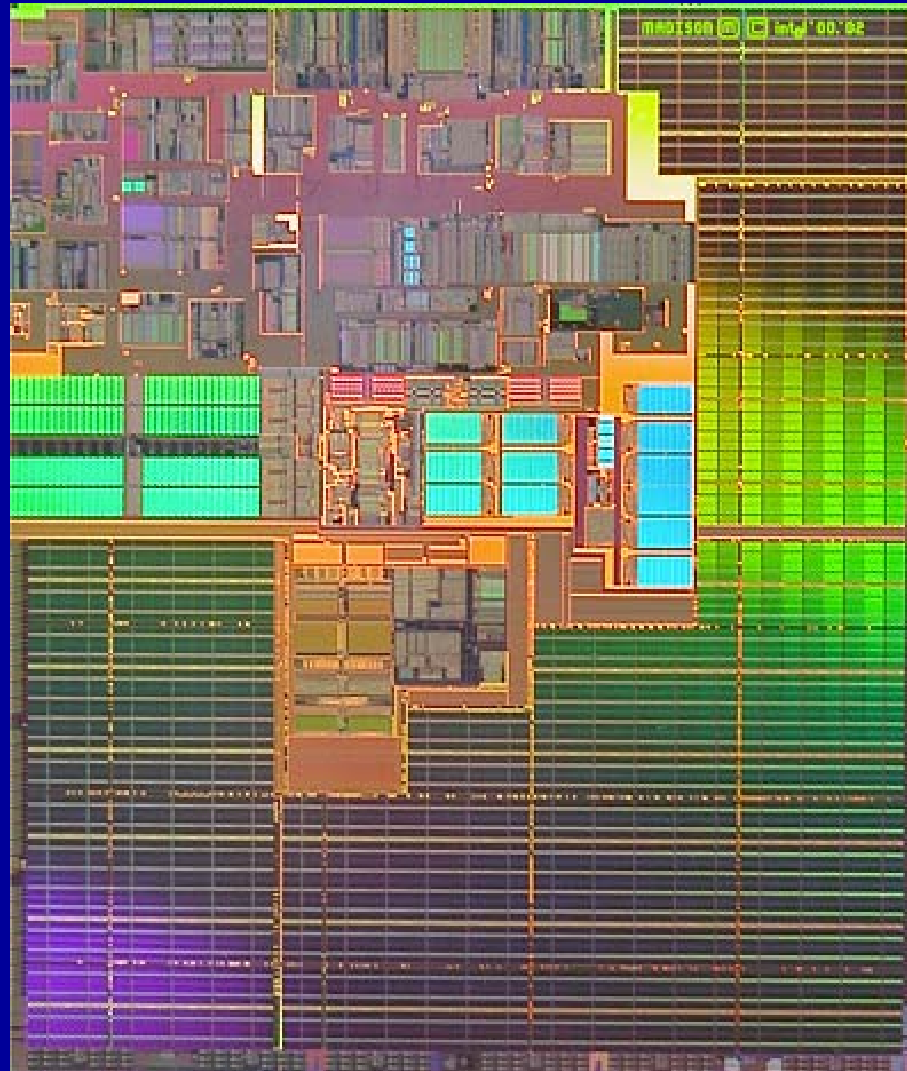


PROGRESS IN MICROELECTRONICS

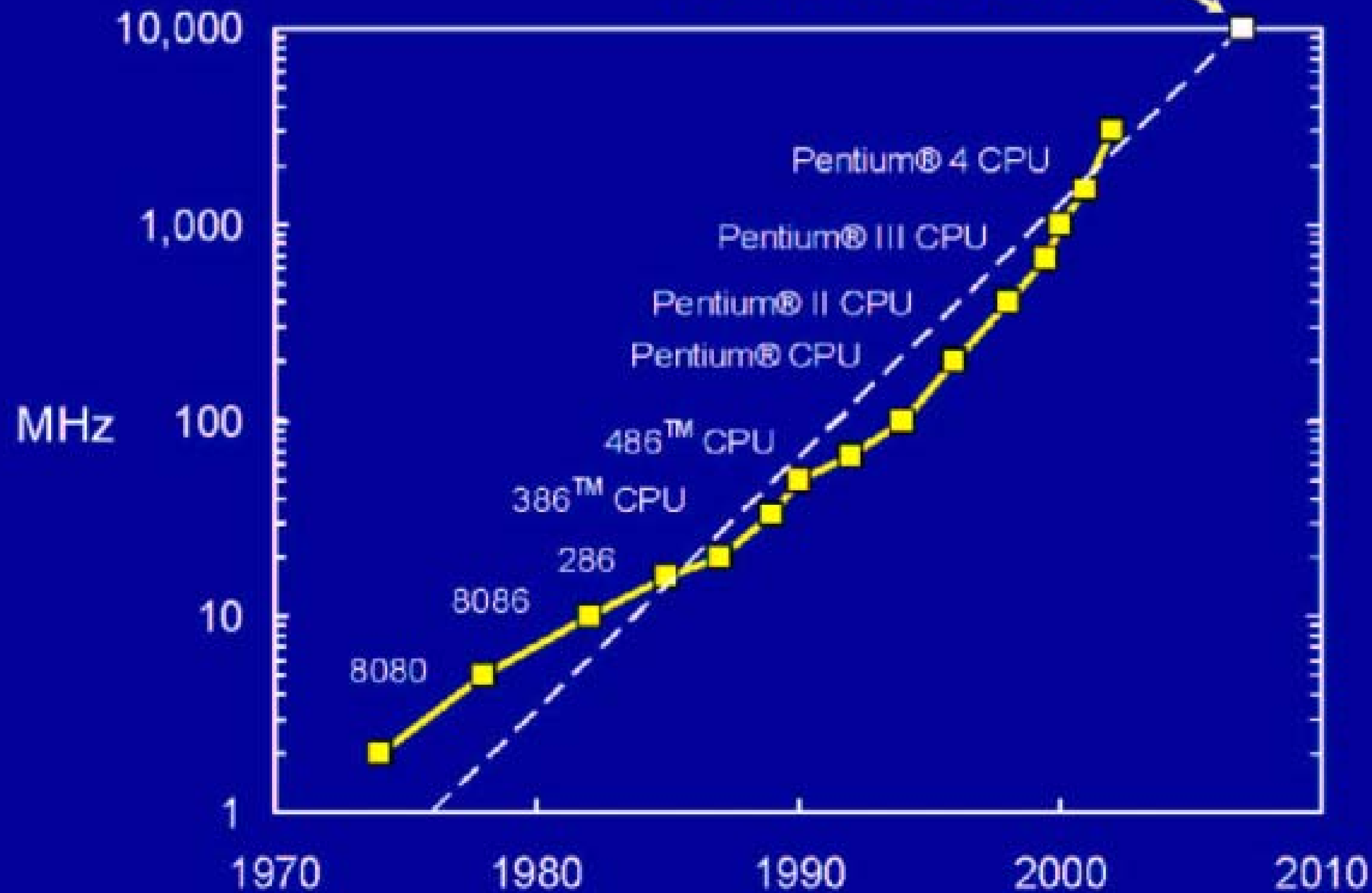
Year	1961	1970-1971	2003	Ratio
Design Rule (μm)	25		0.09	270 ↓
V_{DD} (V)	5		1.2	4 ↓
Wafer diameter (mm)	25		300	12 ↑
Devices per chip	6		8×10^{9}	10^{9} ↑
DRAM density (bit)	–	1k	4G	4×10^{6} ↑
Nonvolatile memory density (bit)	–	2k	2G	10^{6} ↑
Microprocessor clock rate (Hz)	–	750k	3G	4×10^{4} ↑
Transistor shipped / year	10^{7}		10^{18}	10^{11} ↑
Average transistor price ($)	10		2×10^{-7}	5×10^{7} ↓

ITANIUM MICROPROCESSOR

(410 Million Transistors 374 mm^2 0.13µm   1.5 GHz)

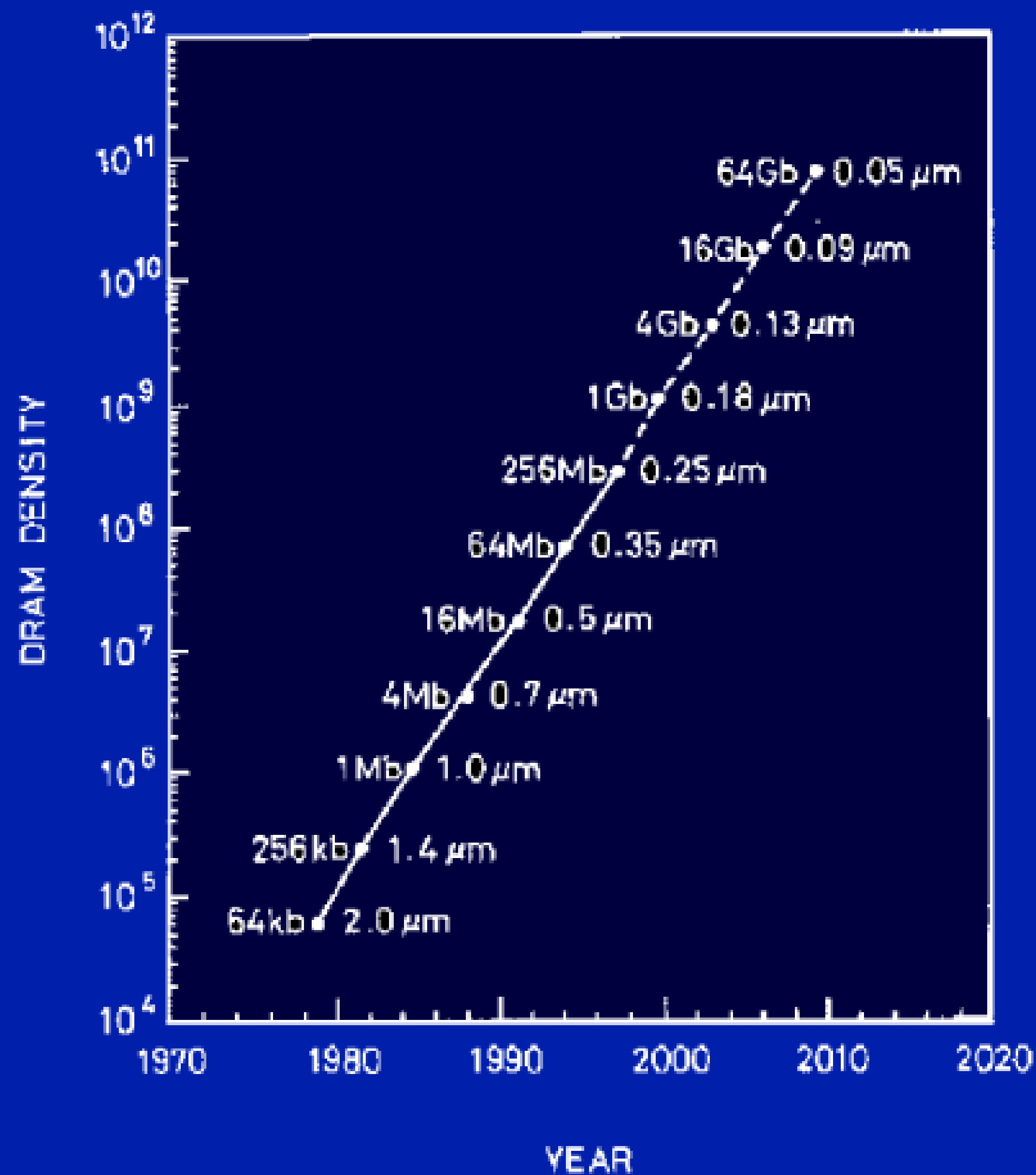


CPU MHz Trend



intel®

MOORE'S LAW



Patented Mar. 7, 1933

1,900,018

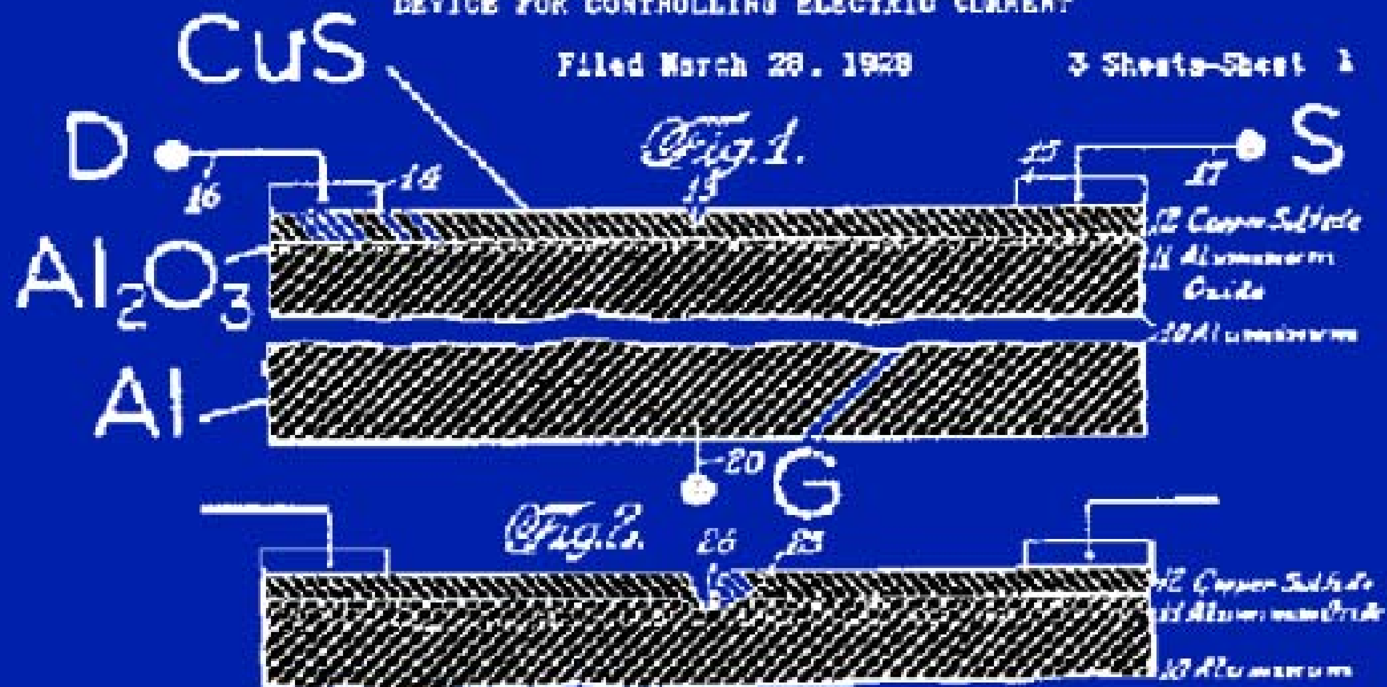
UNITED STATES PATENT OFFICE

JULIUS EDGAR LILIENFELD, OF BROOKLYN, NEW YORK

DEVICE FOR CONTROLLING ELECTRIC CURRENT

Application filed March 28, 1928. Serial No. [illegible]

J. E. LILIENFELD



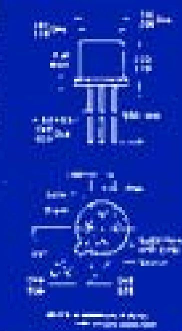
MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor)

FIRST COMMERCIAL MOSFET, 1964

Fairchild Data Sheet for p-Channel MOSFETs

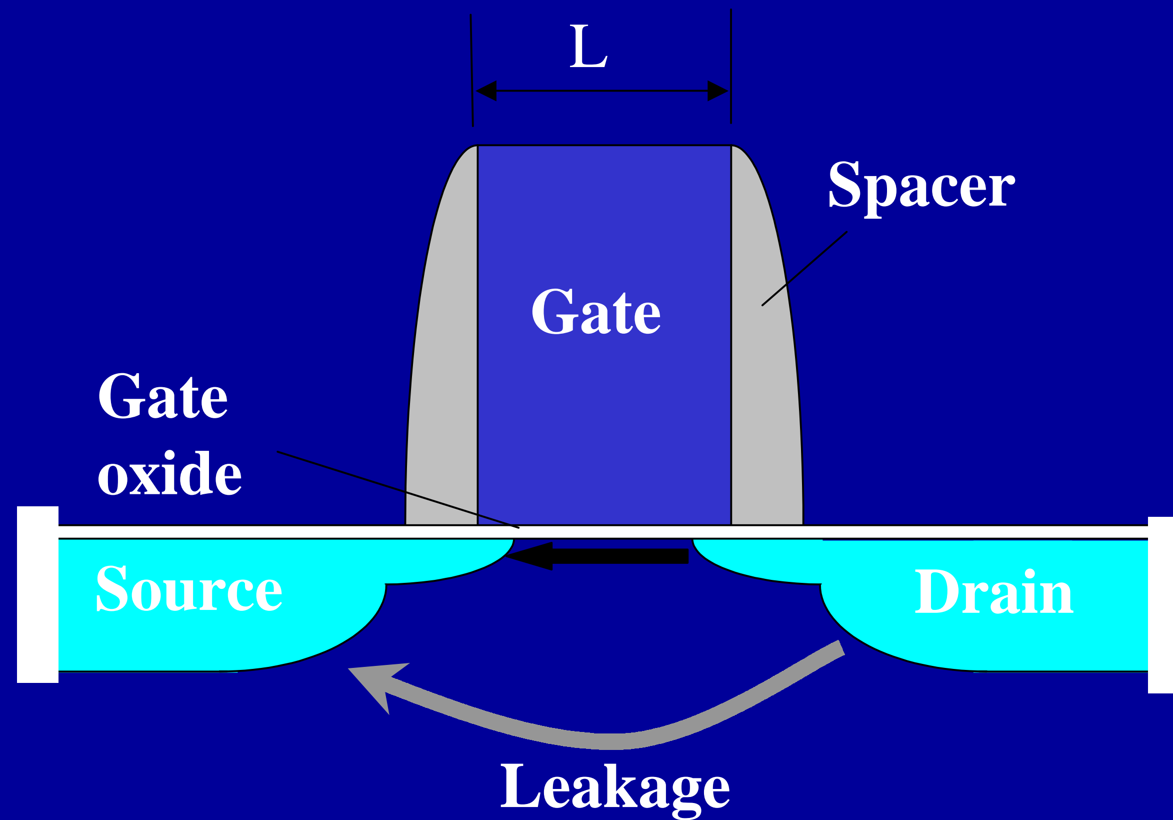
PRELIMINARY SPECIFICATIONS — OCTOBER 1964

PHYSICAL DIMENSIONS



P-CHANNEL MOS FIELD-EFFECT TRANSISTOR — DIFFUSED SILICON PLANAR II DEVICE

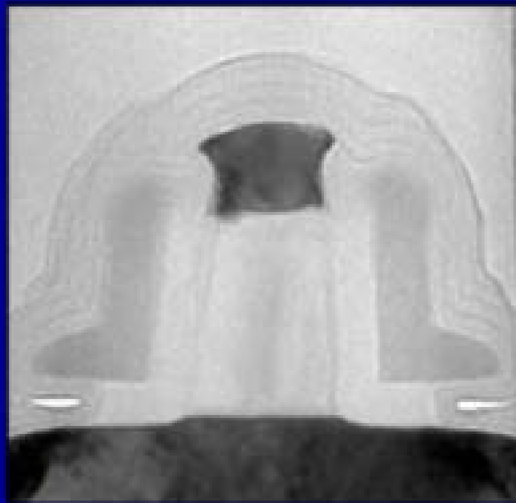
Planar CMOS

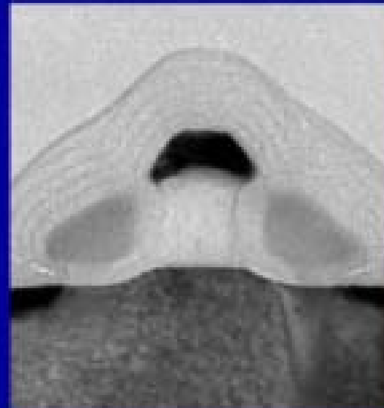


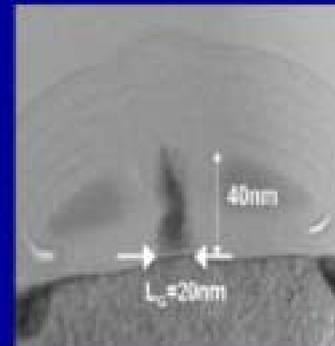
Planar CMOS Transistor Scaling

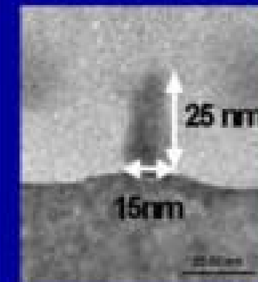
Today

Future



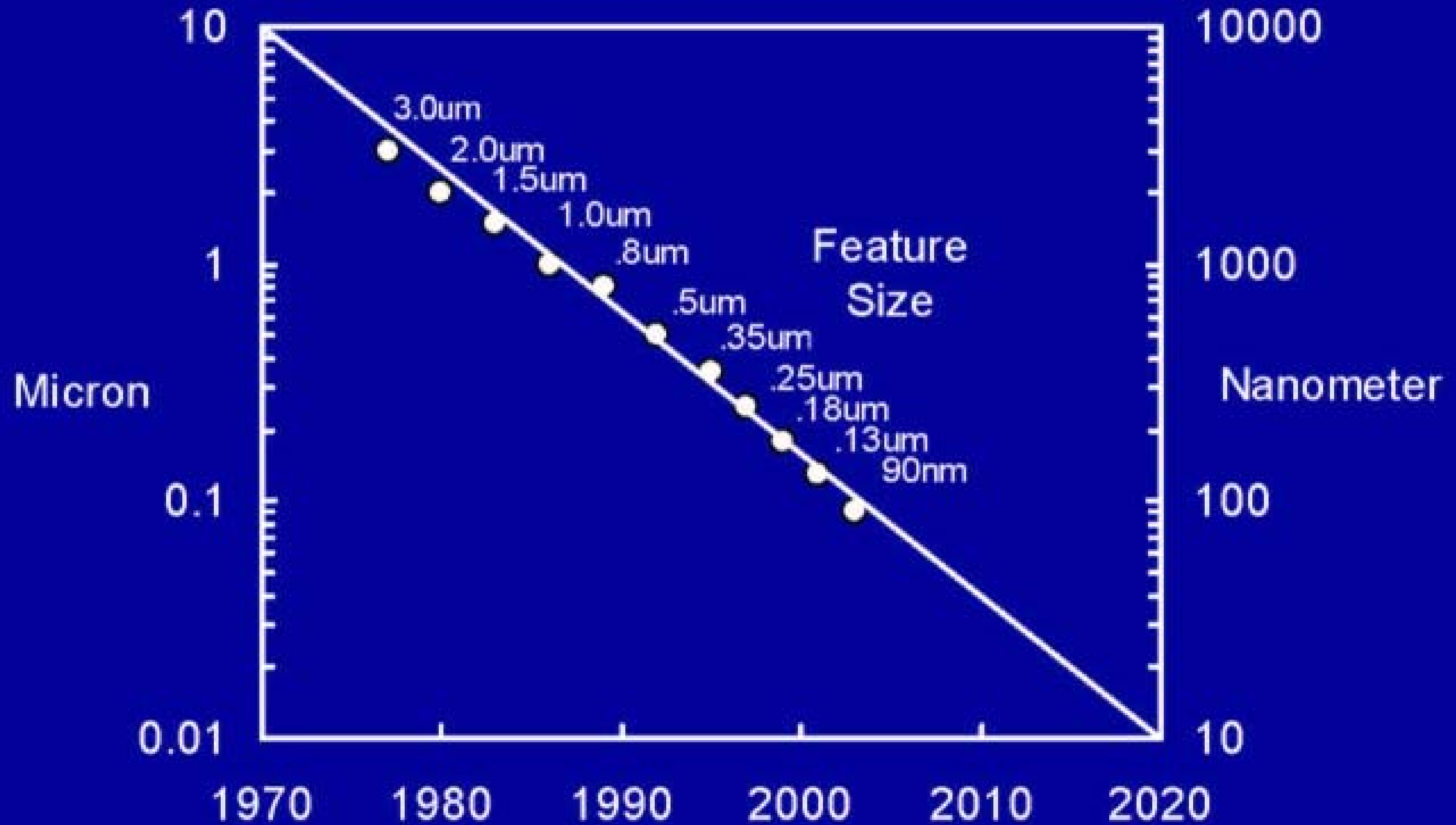




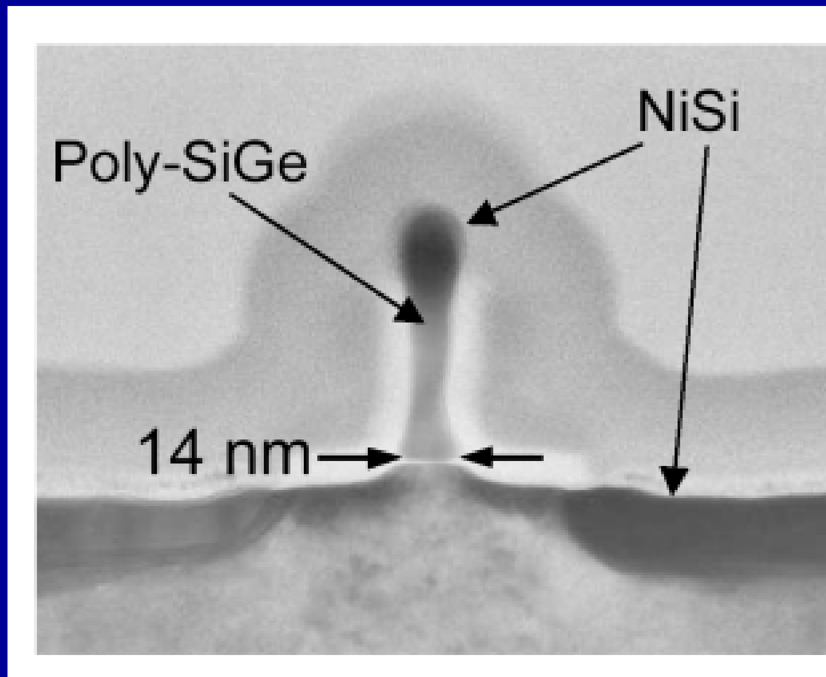


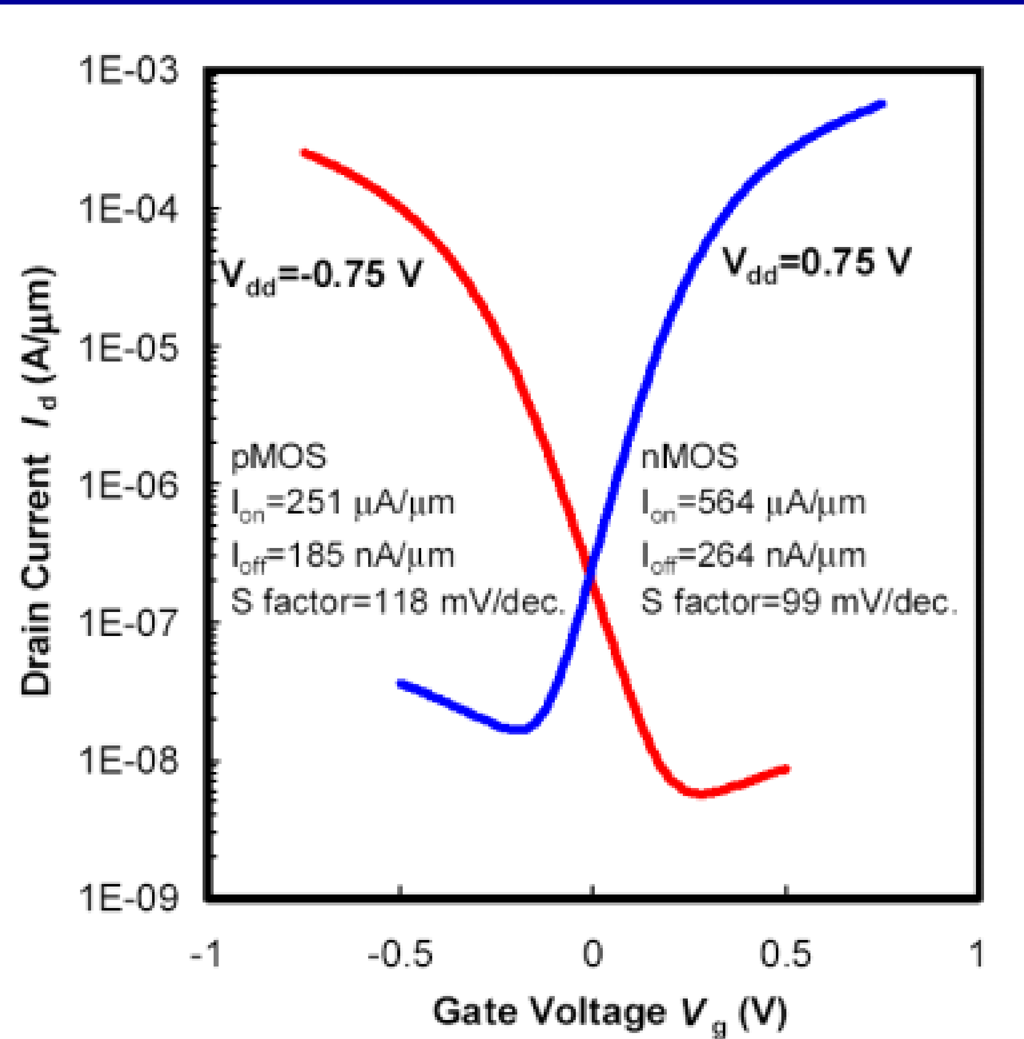
50 nm　　30 nm　　20 nm　　15 nm

Gate Length

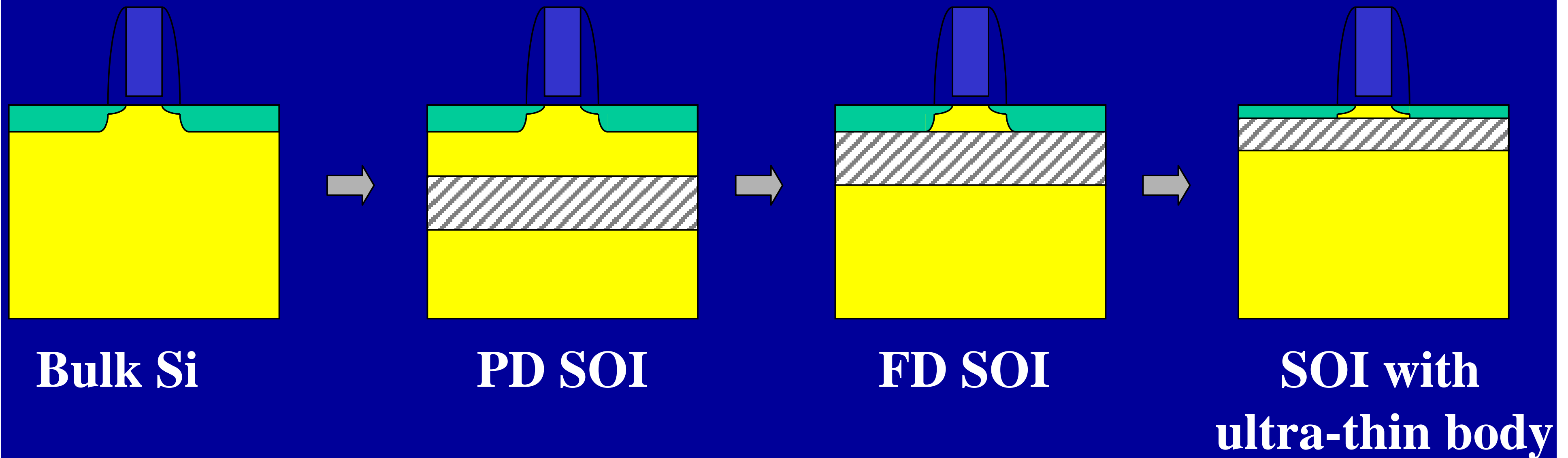

Feature Size Trend
10
1
0.1
0.01
Micron
10000
1000
100
10
Nanometer
3.0um
2.0um
1.5um
1.0um
.8um
.5um
.35um
.25um
.18um
.13um
90nm
Feature
Size
1970
1980
1990
2000
2010
2020

14 nm Gate Length CMOS
(IEDM'2002, S.27.1, p.639)





Evolution of Device Structure

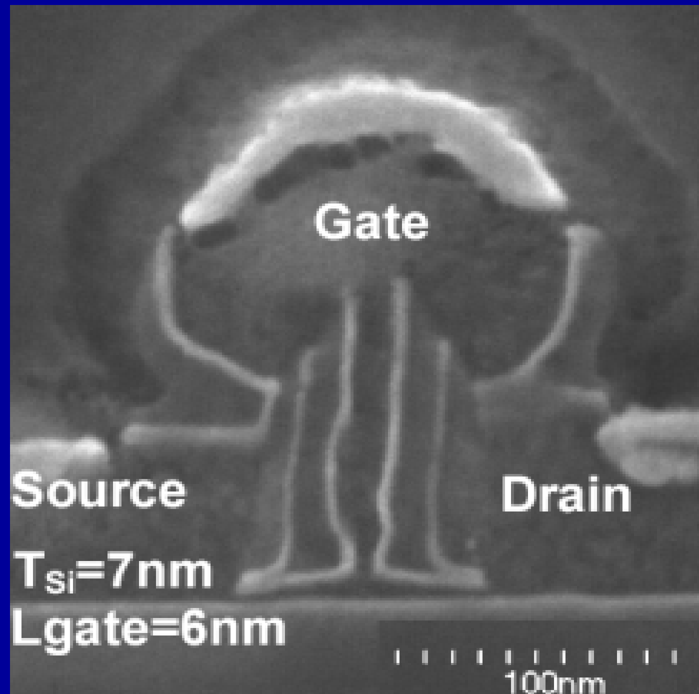


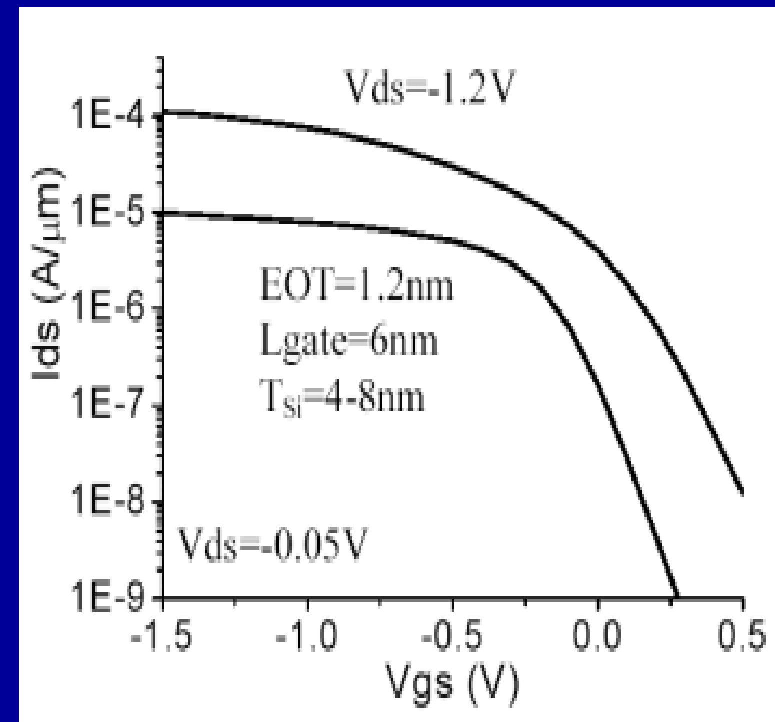
Targets

- Ideal sub-threshold slope
  (~ 60 mV/dec at room temperature)
- High current drive
- Low off current
- Good short-channel effect control
- Non-sensitive to parameter fluctuation

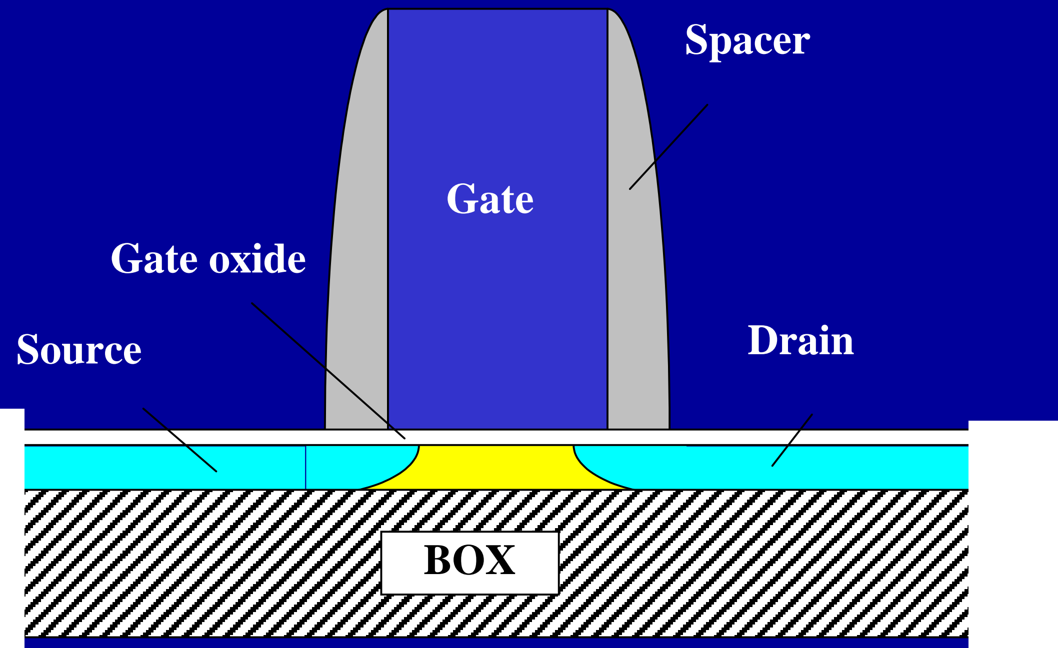
6 nm Gate Length UTB SOI PMOS

(IEDM'2002, S.10.6, p.267)



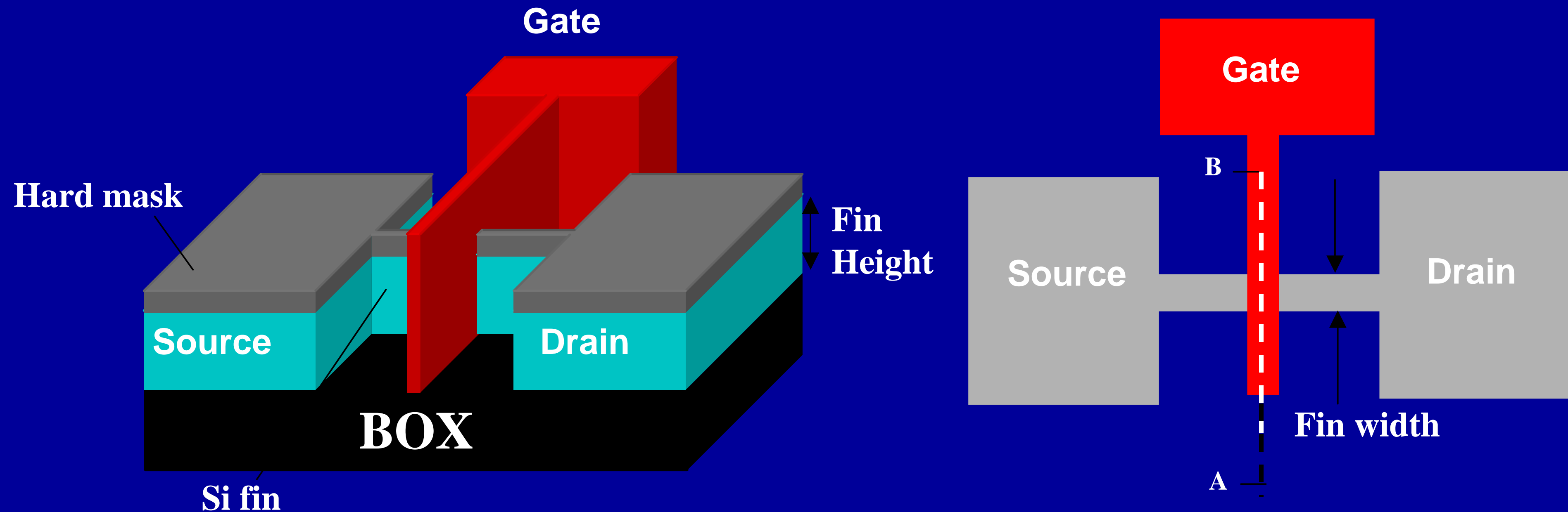


Issues for UTB SOI CMOS



- SCE control T_{SOI}~$1/3L_{min}$
- Parasitic S/D resistance
- Quantum confinement effect
  -Vth increase
- Body thickness fluctuation
  -Vth increase
  -Mobility degradation

Quasi-planar SOI FinFET



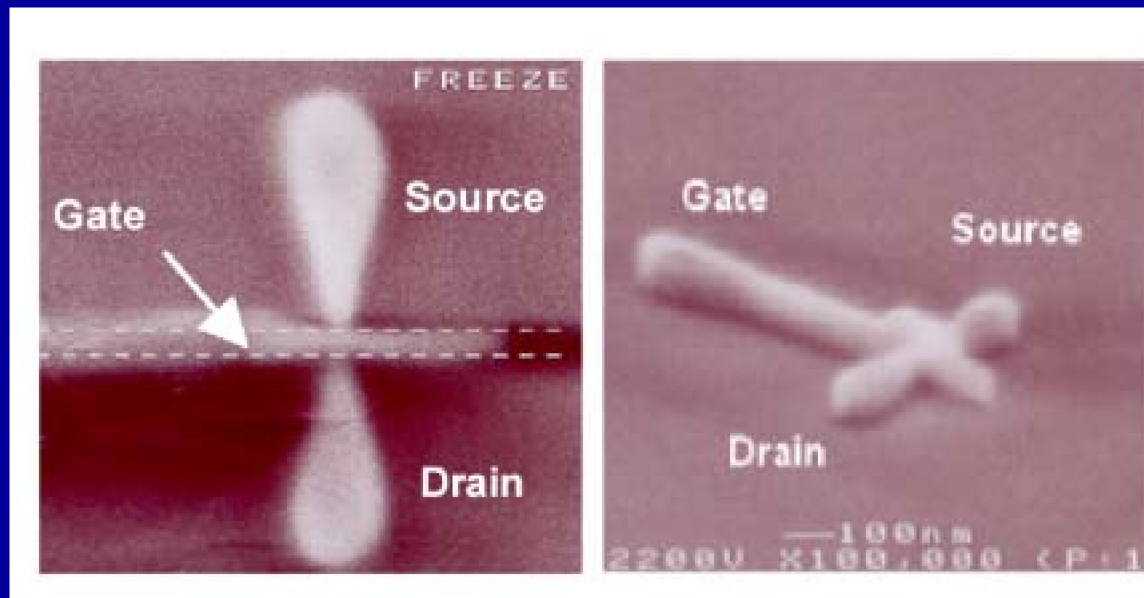
Advantages

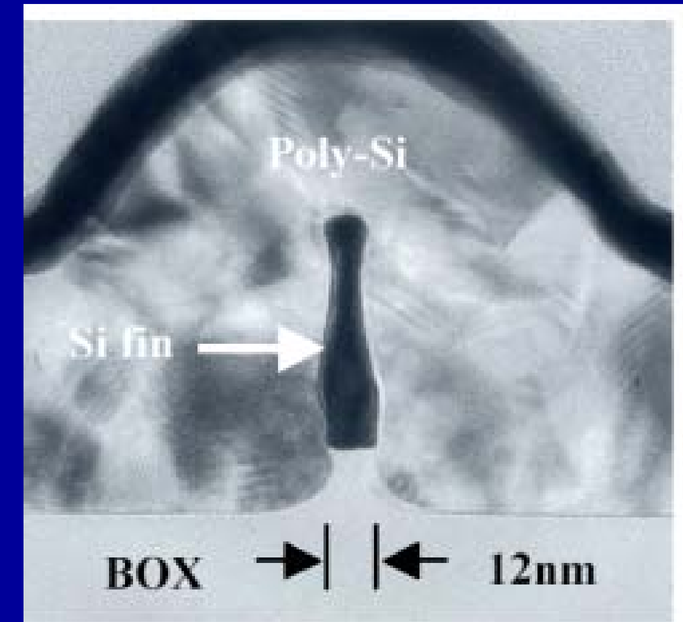
- Relaxed constraint on channel thickness
- Relaxed constraint on EOT
- Improved SCE control
- Compatible with modern manufacturing steps

Issues

- Formation and control of fine Si fins
- Formation and control of sidewall spacer
- Parasitic S/D resistance
- Vth adjustment

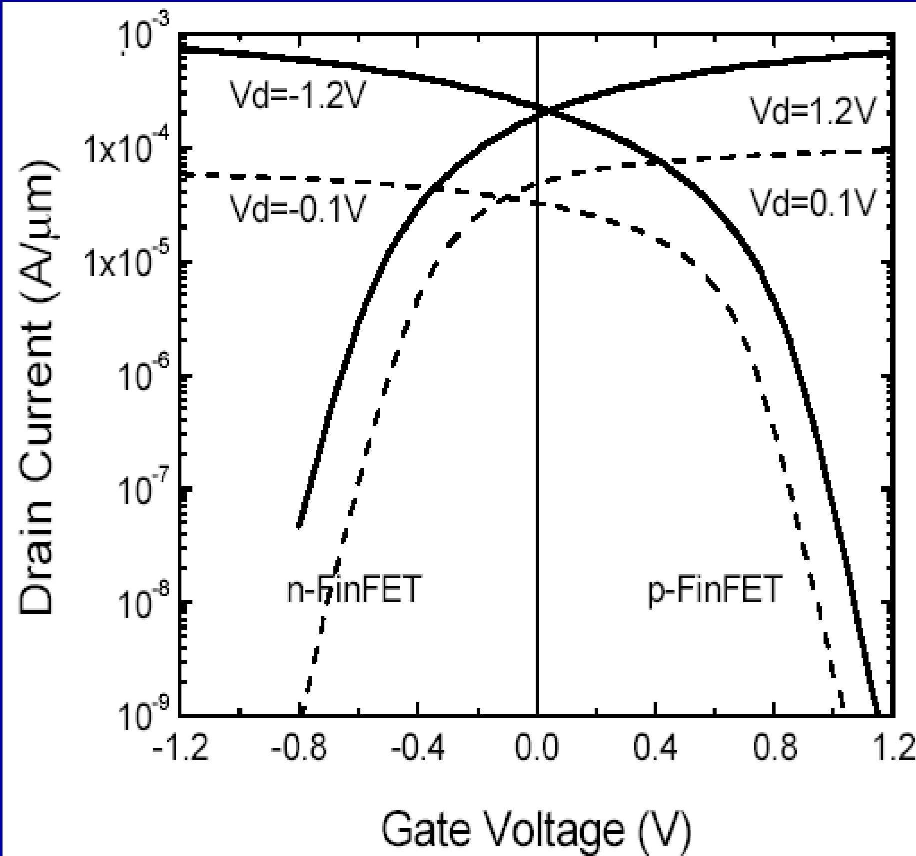
10 nm Gate Length FinFET
(IEDM'2002, S.10.2, p.251)

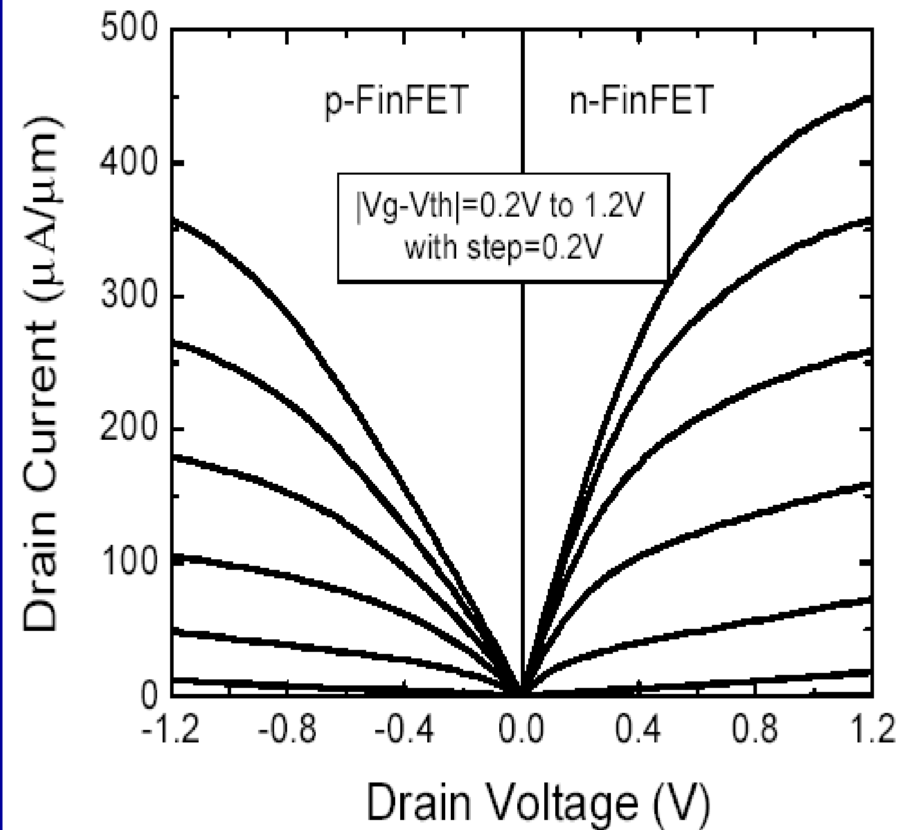




10 nm Gate Length FinFET

(IEDM'2002, S.10.2, p.251)

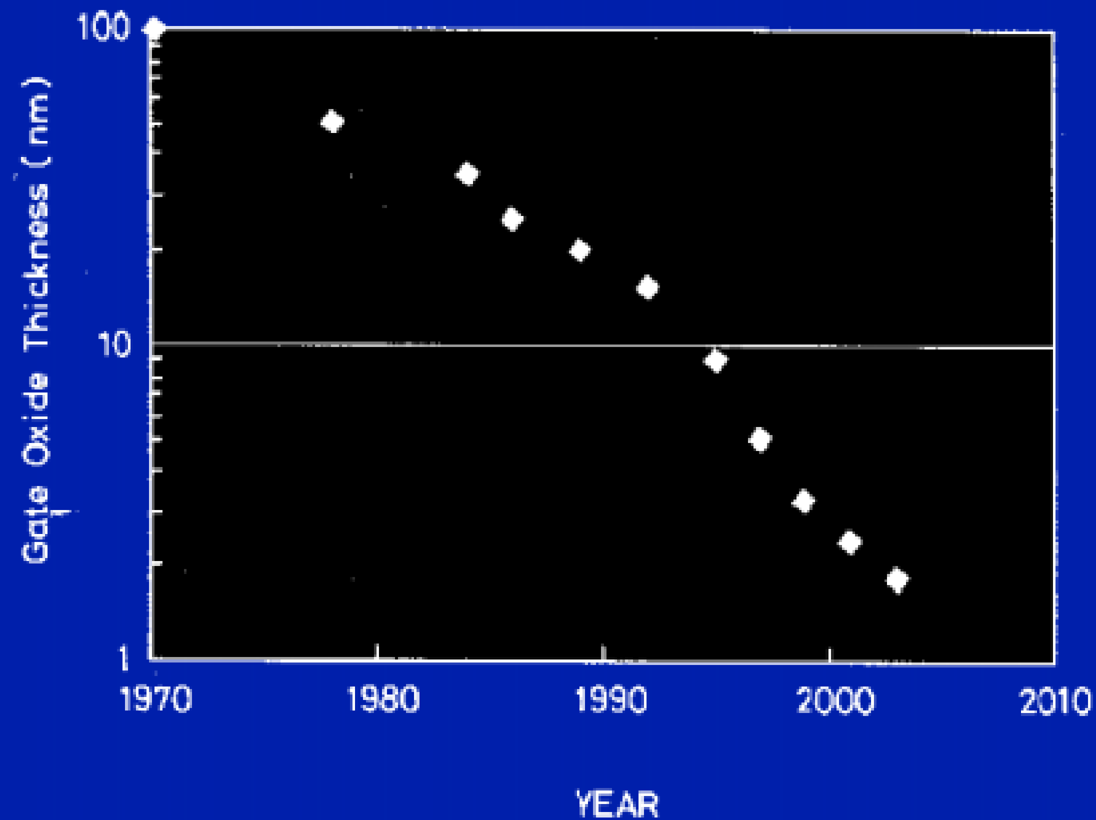


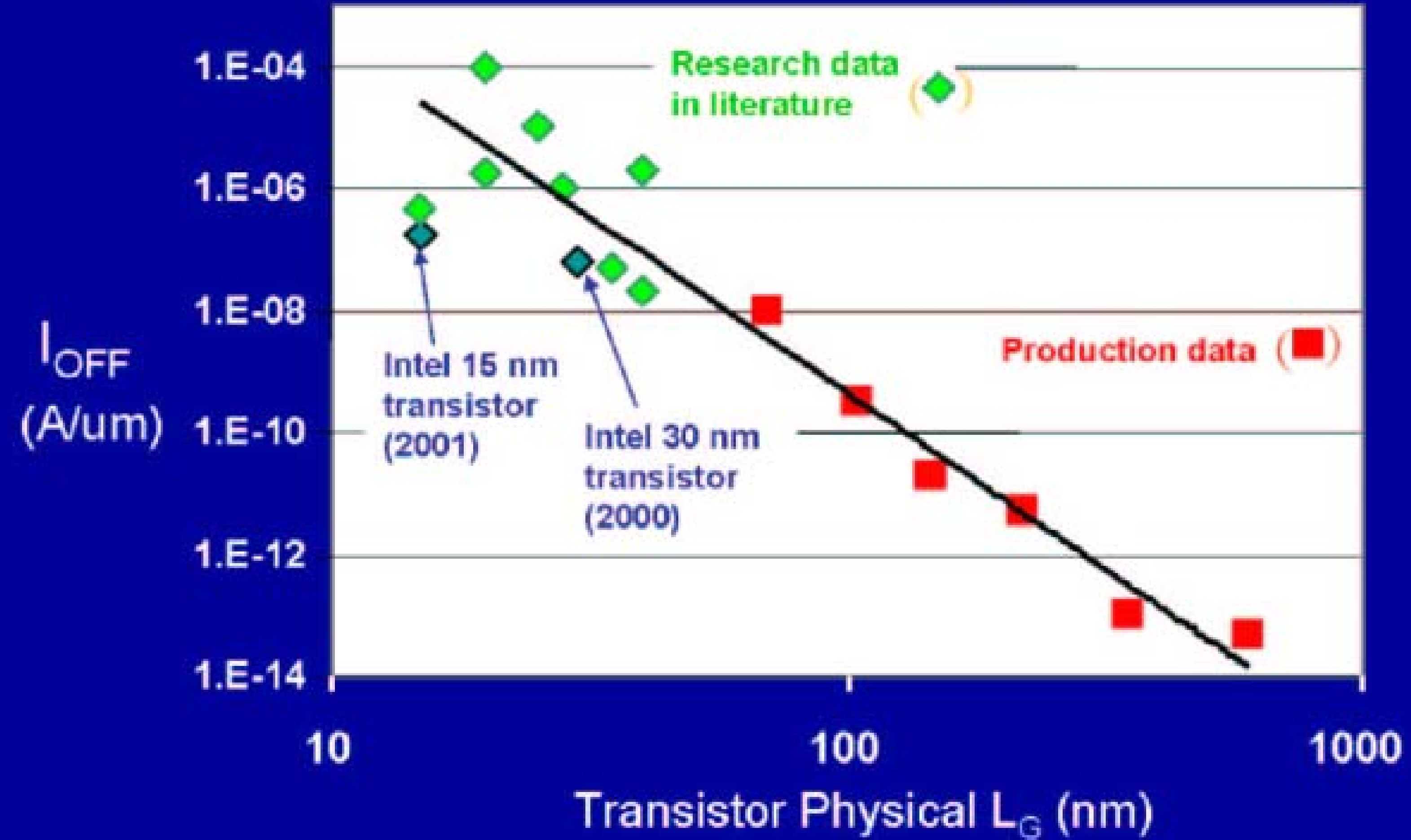


Major Issues for Device Scaling

- Leakage Currents
  - Tunneling currents from gate to channel, body to drain, and source to drain
  - Thermally generated subthreshold channel current
- Fluctuation effects
  - Line edge roughness
  - Film thickness control (channel and gate dielectric)
  - Dopant distribution
- Power Consumption

MOSFET EFFECTIVE DIELECTRIC THICKNESS

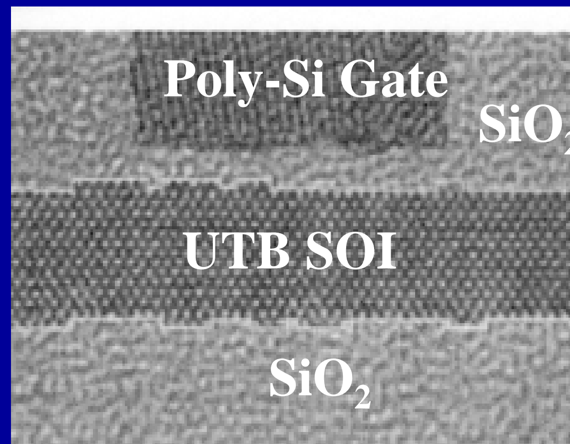



Transistor I_{OFF} Leakage Trend
Research data in literature
Production data
Intel 15 nm transistor (2001)
Intel 30 nm transistor (2000)
I_{OFF} (A/um)
1.E-04
1.E-06
1.E-08
1.E-10
1.E-12
1.E-14
10
100
1000
Transistor Physical L_G (nm)

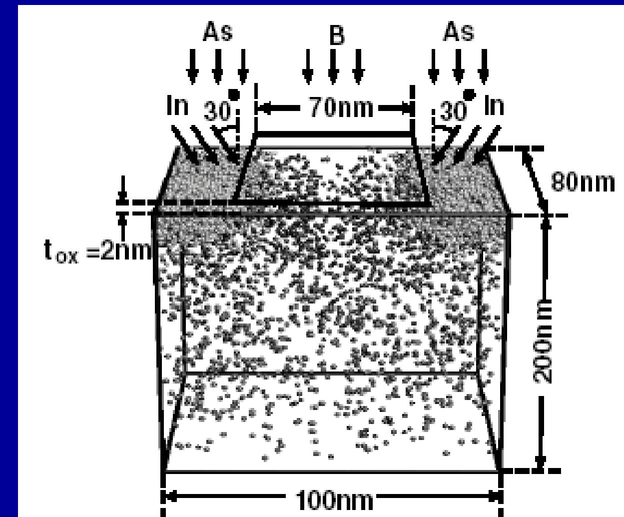
Fluctuation Effects

Line width

Film Thickness

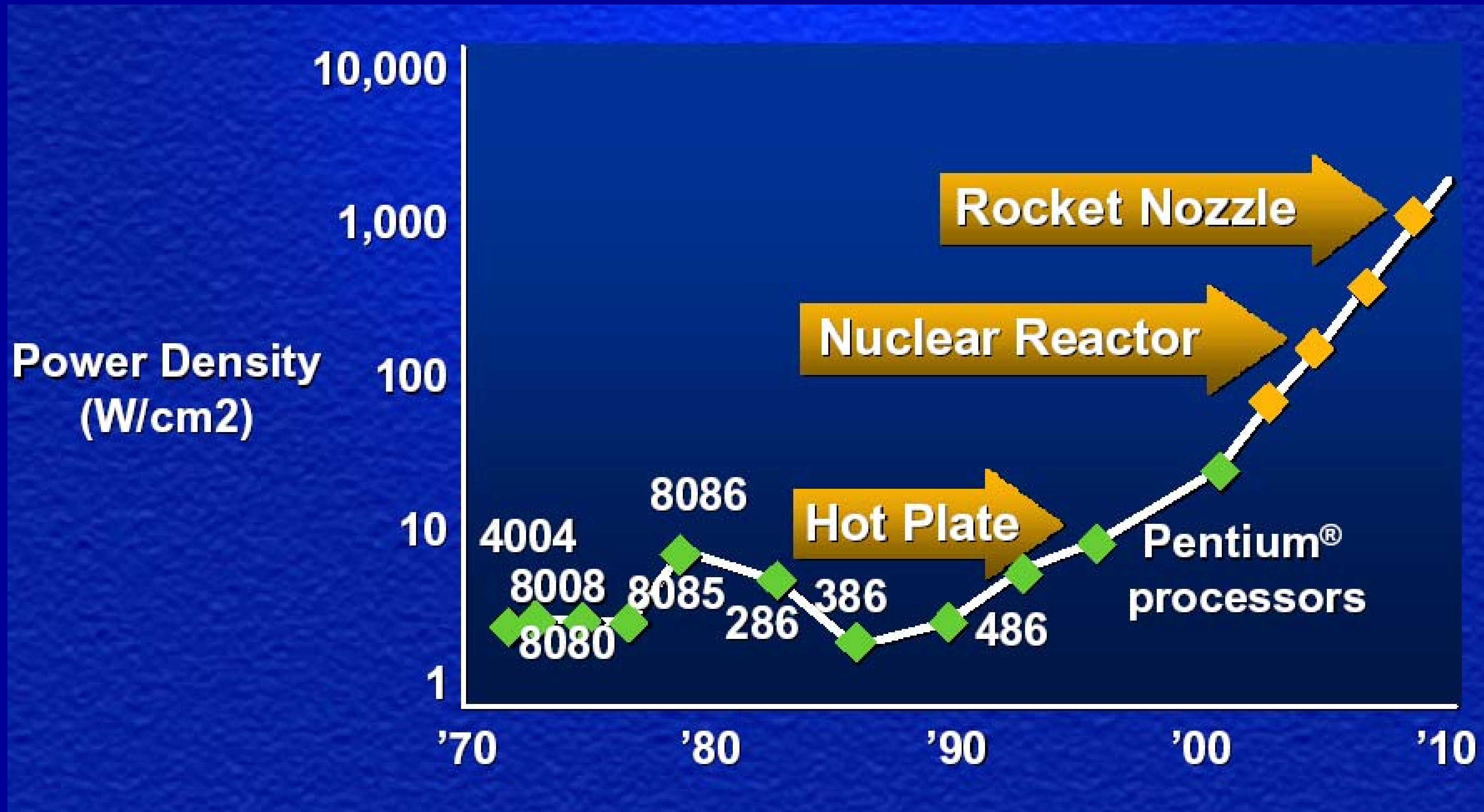


Dopant concentration

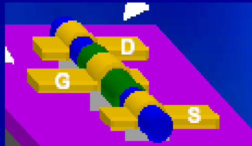


Power Density Will Get Even Worse

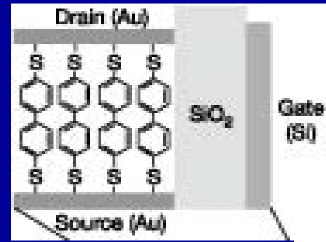
(Andrew S. Grove, Luncheon Talk in IEDM'02)



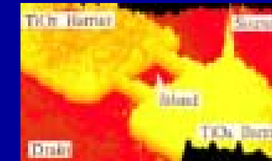
Nanoelectronic Devices Options



Carbon Nanotube (CNT)



Molecular Devices


Single electron transistor (SET)

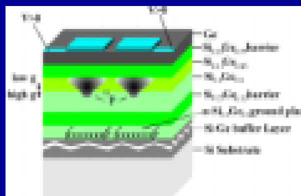
Which can replace Si CMOS?

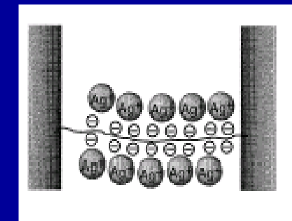
Targets:

Lower cost

Less power consumption

Higher performance


Spintronics


DNA IC

Requirements for Nanotechnology Options

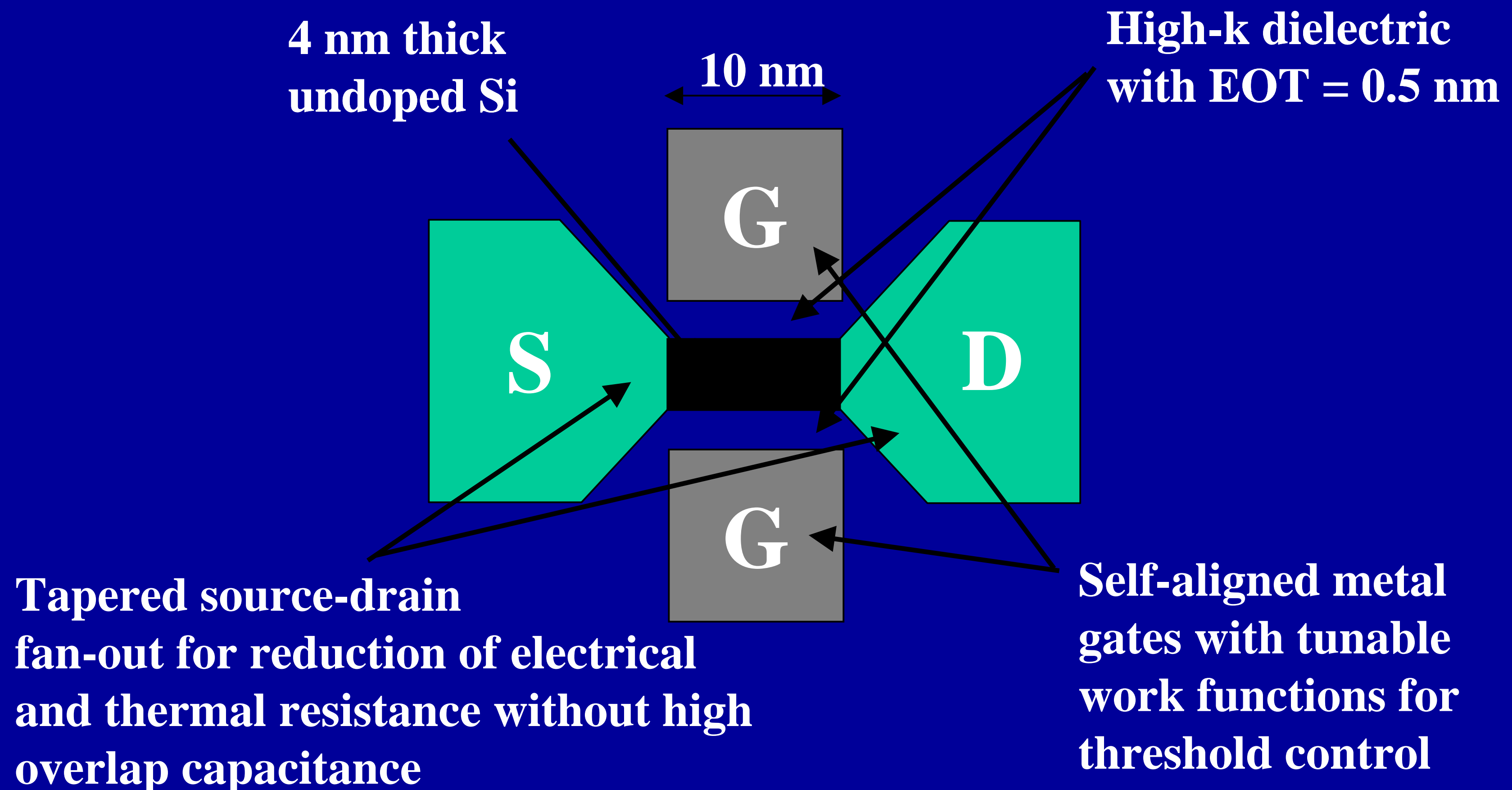
- Feature size < 10 nm
- High energy conversion efficiency
- High speed
- Room temperature operation
- Good stability, uniformity and reliability

NANOTECHNOLOGY OPTIONS

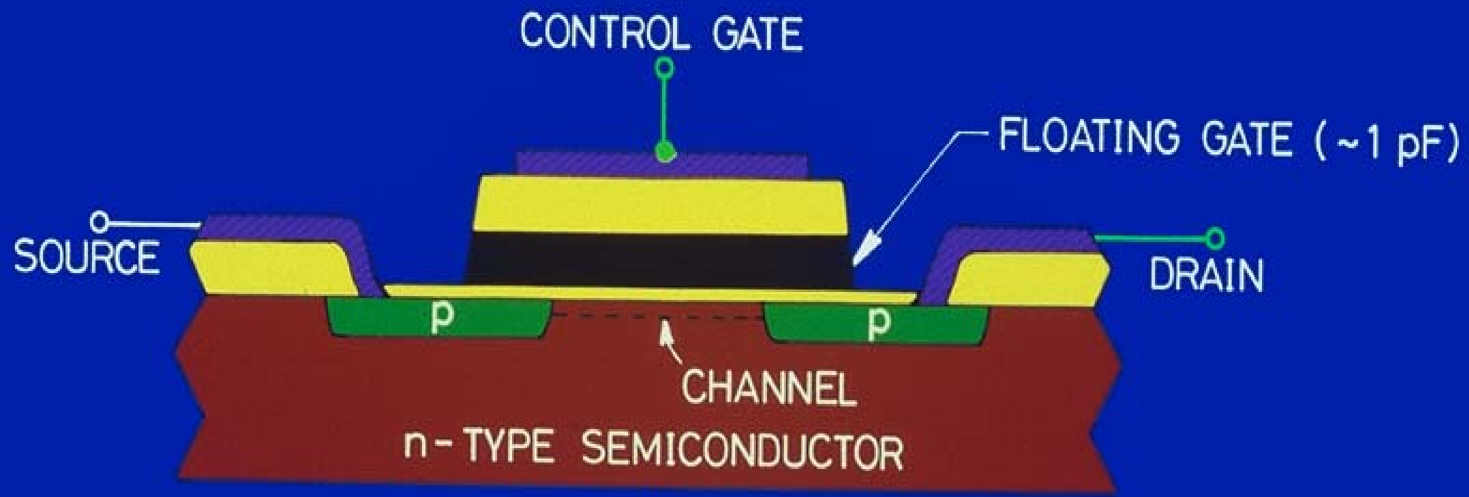
- Carbon-nanotube FET
  - difficulty of forming low resistance contact
  - difficulty in forming nanotubes with the desired physical features
  - how to position nanotubes in a given position in a cost-effective way
- Molecular Devices
  - limitation in operating temperature
  - difficulty in making contact to individual molecules
- Quantum-dot Cellular Automata (Single-electron Parametron)
  - limitation in operating temperatures
  - sensitivity to random background charge
  - slow speed
  - difficulty in transmitting signals across larger intra-die distances

The Ultimate MOS Transistor

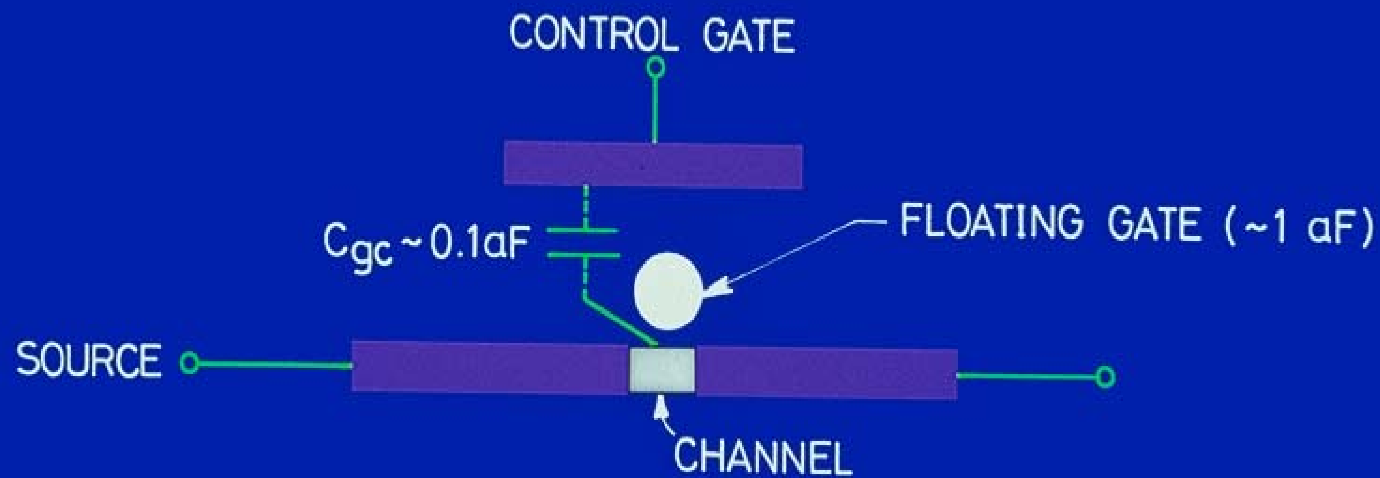
(Y. Taur, in short course program of IEDM'01)



(ITRS'2001, 2016, 25 nm-node, physical gate length for MPU: 9 nm)

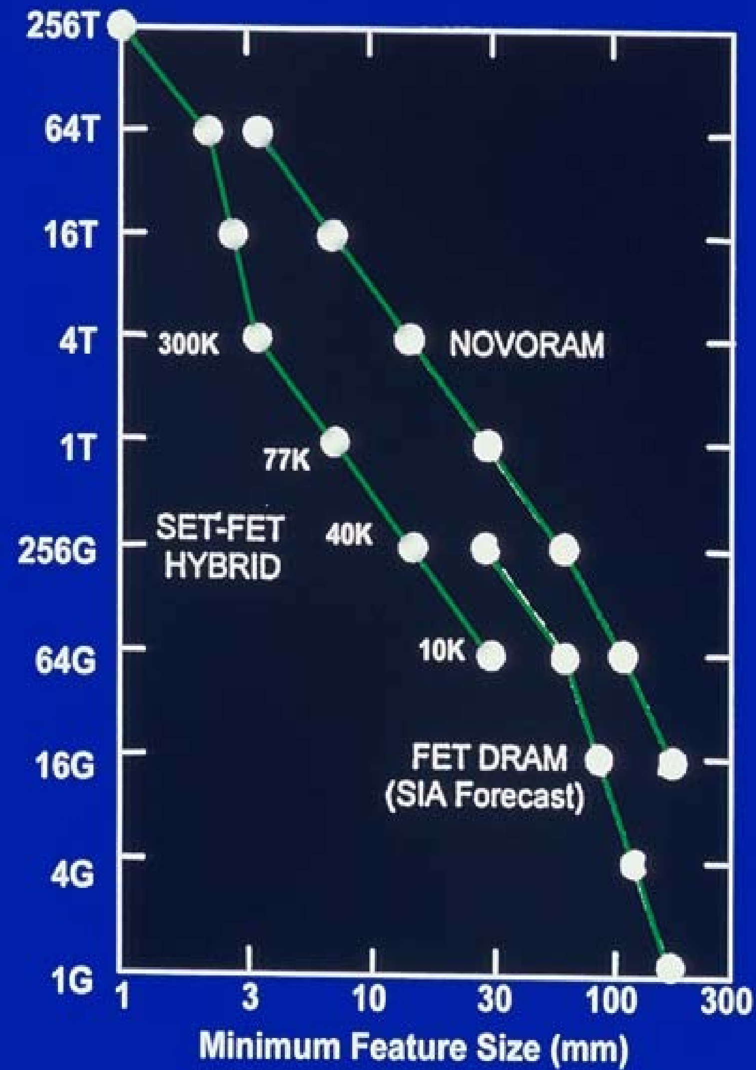


(a)



(b)

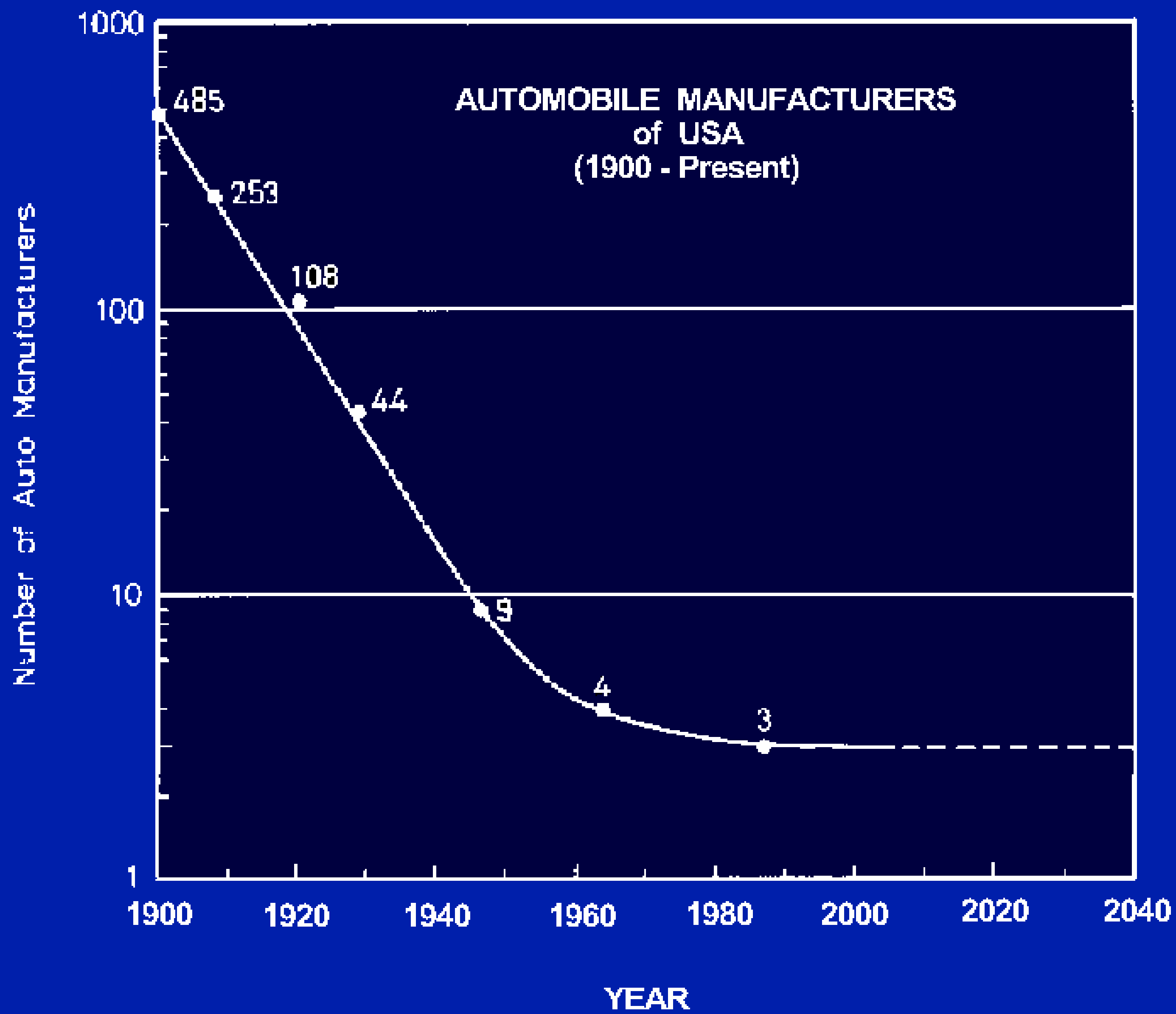
MEMORY DENSITY OF DRAM AND SET



APPLICATIONS AT THE SCALING LIMIT

Application	Memory (GB)	Comp. Rate (GIPS)	Power / DSP (W)	Si Area (cm^2)
Speech recognition (to text)	0.01-0.1	0.1-1	0.001	0.1
Real time language translation	0.1	1-10	0.01	0.2
Video encoding, very high res. (1920 ×1200, 30 fps)	0.01	20-200	0.2	0.6
2-way video wrist watch	0.01	0.05	0.0002	0.01
PDA	0.1	1-10	0.01	0.2
Factoring 512 bit numbers	1	4000	10	40
Deep Blue chess	3	10000	3	100
QM-based device simulation+	10	100	30	15
PetaFLOPS computing challenges+	3×10^4	10^6	10^6	5×10^4

+ Power based on general-purpose processor applications instead of DSP



AUTOMOBILE MANUFACTURERS
of USA
(1900 - Present)
Number of Auto Manufacturers
1000
100
10
1
485
253
108
44
9
4
3
1900
1920
1940
1960
1980
2000
2020
2040
YEAR

CONCLUSION

- Major issues for device scaling are leakage currents, fluctuation effects,and power consumption

- The double-gate SOI MOSFET is a promising candidate for the ultimate device structure, its gate length can be scaled down to 10 nm

- There are numerous applications of MOSFET at the scaling limit (around 2015) , and silicon technology is expected to continue as the most powerful driver of the Information Age