Designing the First Superconductor RSFQ Chipset for a 32-bit Floating-point Vector Multiply Unit

Mikhail Dorojevets and Dmitri Strukov
Dept. of Electrical and Computer Engineering, SUNY–Stony Brook, USA

We present the architecture and gate level design of a 32-bit floating-point vector multiply unit with a target clock frequency of 25 GHz in the rapid single flux quantum (RSFQ) logic. This multiplier is a core processing component of a multiple chip vector processing unit being developed within the FLUX-2 project by a team including SUNY Stony Brook, Northrop Grumman Space Technology (NGST), and the Jet Propulsion Laboratory (NASA). Our goal is to design a dual-chip multiplier capable of calculating one 32-bit floating-point result per 40 ps cycle, while processing two input streams of data encoded in the IEEE 754 single precision format from vector register memory on a separate chip. All data transfers between chips placed on a multi-chip module are to be done over superconductor Nb transmission lines at a 25 GHz transmission rate, i.e., the same clock rate used to process and read/write data inside the chips.

Our current project is the next evolutionary step for superconductor technology. It is based on the experience with the design, fabrication, and testing of an 8-bit FLUX-1 RSFQ microprocessor,[1] and the revolutionary NGST's work on 60 Gbps chip-to-chip communication.[2] All the chips will be implemented with NGST's new niobium tri-layer low-temperature superconductor technology, which allows fabrication of 1.25 μm Josephson junctions (JJs) with 8KA/cm^2 critical current density.[3] We expect each chip to have a ~100 mm^2 die, which would allow us to have up to 100K JJs, or 10K RSFQ gates per chip.

We examine several RSFQ design options for multiplication, including encoding schemes and topologies used to generate and reduce partial products. We show how the peculiarities of the RSFQ logic, such as high broadcast penalties and the low fan-out of RSFQ gates, together with the high data/clock skew unavoidable in the multi-chip 25 GHz vector multiply unit force designers to modify well-known ideas and develop new modular approaches to fast floating-point multiplication in superconductor processors.

This work is supported by DoD.

---

1 M. Dorojevets, and P. Bunyk. "Architectural and implementation challenges in designing high-performance RSFQ processors: FLUX-1 microprocessor and beyond", to appear in *IEEE Trans. Appl. Supercond.* (2003).

2 Q. P. Herr, A. D. Smith, and M. S. Wire, "High-speed data link between digital superconducting chips", Appl. Phys. Lett. **80**, 3210 (2002).

3 A. Kleinsasser, A. Silver, L. Abelson, *et al.*, "Superconductor electronics technology for high performance computing", to appear in *Abstracts ISEC-03*, Australia, July 2003.