FLUX-1: the first superconductor 20-GHz 8-bit RSFQ microprocessor built in 1.75-μm Nb-trilayer technology

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We will describe the first single-chip superconductor microprocessor [1] designed in rapid single-flux-quantum (RSFQ) logic [2] at SUNY Stony Brook and fabricated using TRW's LTS 4 kA/cm^2, 1.75-μm Nb-trilayer technology. A FLUX-1 chip is being developed by a multi-disciplinary collaboration of two design teams at SUNY Stony Brook and a fabrication team at TRW, Inc as a spin-off of the HTMT (Petaflops) project. The goal of the 18-month FLUX project is to find out whether it would be feasible to build full-fledged 50-GHz multithreaded RSFQ processors [3] in a 0.8-μm process (yet to be developed) based on our experimental results with the available 1.75-μm LTS technology.

Each FLUX-1 chip represents a simple 8-bit 2-way long-instruction-word (LIW) microprocessor with a pipelined instruction memory of 30-bit instructions, decode and issue units, 8 integer ALUs interlaced with 8 registers, and input/output ports through which two FLUX-1 chips can communicate with each other at a 5-GHz communication rate over a multi-layer superconductor Nb MCM. The FLUX instruction set consists of ~25 instructions. High performance is reached with a scalable design featuring:

- a very high clock rate;
- localized, regular and ultrapipelined processing in registers with very short wires; and
- instruction-level parallelism utilization with bit-level resolution of data hazards.

A FLUX-1 processor consists of ~55,000 Josephson junctions on a ~12.0x10.6 mm chip with 22 5-GHz, 56 low frequency, and 16 dc solder bump pads. The fabrication of a FLUX-1 chip is planned on May-June 2001. Our estimates and experiments with several test chips fabricated to date show that the processor will be able to operate at clock frequencies close to 20 GHz.

[1] M. Dorojevets, P. Bunyk, and D. Zinoviev, "FLUX chip: design of a 20-GHz 16-bit ultrapipelined RSFQ processor prototype based on 1.75-um LTS Technology", to be published in *IEEE Trans. Appl. Supercond.* (2001).

[2] K. K. Likharev, and V. K. Semenov, "RSFQ logic/memory family: a new Josephson-junction digital technology for sub-terahertz–clock-frequency digital systems", *IEEE Trans. Appl. Supercond.* **1**, 3 (1991).

[3] M. Dorojevets, "COOL multithreading in HTMT SPELL-1 processors", *Intl. J. High Speed Electron.Sys.* **10**, 247 (2000).