A Field-Effect Transistor with a Negative Differential Resistance

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Abstract—**We report the effect of negative differential resistance (NDR) in the drain circuit of a new type of selectively doped AlGaAs/GaAs heterojunction transistor. The key new element of our structure is the presence of a subsidiary GaAs conducting layer, separated from the FET channel by an AlGaAs graded barrier. In this work the subsidiary layer is realized by the conducting substrate. The NDR effect arises due to the heating of channel electrons by the source-to-drain field, and the subsequent charge injection over the barrier. This effect is strongly influenced by the gate and substrate voltages. In a floating-substrate arrangement the current–voltage characteristics exhibit memory effects associated with retention of injected charge in the substrate. In this mode, the NDR is seen only at low temperatures with the peak-to-valley ratios in current at 77 K reaching values as high as 30. On the other hand, when the substrate is biased positively, the NDR results from a peculiar effect of dynamical channel depletion by the injected space charge which drifts on the downhill slope of the graded barrier. In this case, the NDR is observed even at room temperature.**

IN A RECENT PAPER [1][1], we proposed a new device concept based on hot-electron transfer between two conducting layers in a AlGaAs/GaAs heterostructure. One of these layers is an FET channel, and it is separated from the second layer by a graded $Al_xGa_{1-x}As$ potential barrier. Application of a source-to-drain field causes heating of channel electrons and an exponentially enhanced charge injection into the second layer. This phenomenon was expected to produce a strong negative differential resistance (NDR) in the drain circuit. The proposed device received the name NERFET, which stands for *ne*gative *r*esistance *f*ield-*e*ffect *t*ransistor.

Fig. 1 shows the device structure and its band diagram. It has been grown by molecular-beam epitaxy (MBE) on Si-doped (10^{18} cm^{-3}) GaAs substrate, which plays the role of the second conducting layer. We used a {100} substrate orientation and a 640°C growth temperature with arsenic-rich growth conditions and conversion of the arsenic beam from As_4 to As_2. The growth sequence commenced with a 1-μm homoepitaxial layer of Si-doped ($\sim 10^{18}$ cm^{-3}) GaAs. The content of aluminum in the undoped barrier layer of thickness $l = 1450$ Å was graded from $x = 0.11$ to $x = 0.34$ by progressively increasing the aluminum molecular-beam cell temperature during growth of the layer. The upper GaAs conducting channel layer of thickness $d = 190$ Å was undoped. The $Al_{.34}Ga_{.66}As$ layer which provided the conduction

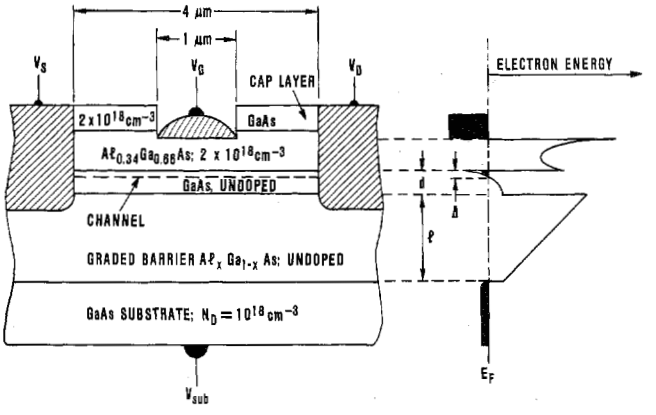

Fig. 1. NERFET structure and energy band diagram. Regions, where the electron gas is degenerate are indicated in black on the band diagram. Dimensions: $l = 1450$ Å, $d = 190$ Å. The content of aluminum in the barrier is graded from $x = 0.11$ to $x = 0.34$.

electrons to the channel contained $\sim 2 \times 10^{18} cm^{-3}$ silicon atoms, was 390 Å thick, and was separated from the channel by an 80-Å-thick undoped $Al_{.34}Ga_{.66}As$ spacer layer.

For NERFET operation, it is essential that source and drain contacts to the channel were insulated from the second conducting layer. We used a Au/Ge-Ag-Au alloy which is known to give shallow (~2000 Å) and abrupt ohmic contacts. We sought to have the bottom edge of contact penetration stop near the top of the graded barrier. To this end we used a thick (1400-Å, silicon-doped) GaAs cap layer (making the total thickness of the structure above the graded barrier about 2100 Å), and experimented with different alloying cycles and temperatures. Best results were obtained by alloying at 420°C for 20 s. Fig. 2 shows the resultant current-voltage ($I_{SUB} - V_{SUB}$) curves in the substrates circuit (source and drain grounded) at 300 K(Fig. (2(a)) and 77 K (Fig. 2(b)). These are typical rectifying characterisitcs of a one-sided triangular barrier of approximate height 0.4 eV [2]. We observed no ohmic leakage down to $I_{SUB} \sim 10^{-10}$ A.

Devices were isolated from one another by selectively removing the conducting material between individual transistors and covering the resultant mesa pattern by silicon nitride. Active device area was cut into the nitride by a CF_4/O_2 plasma etch. Gates were deposited after a self-aligned chemical etch through the cap layer. The gate was notched a little into the AlGaAs layer to produce a slight channel depletion and to ensure concentration of the source-to-drain field in the normally-on device. The gate (notch) length was 1 μm, while the total separation between source and drain was 4 μm; we used 250-μm-wide gates.

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[1] This paper contains an extensive list of references to the work of the University of Illinois group which pioneered the study of real-space hot-electron transfer effects.

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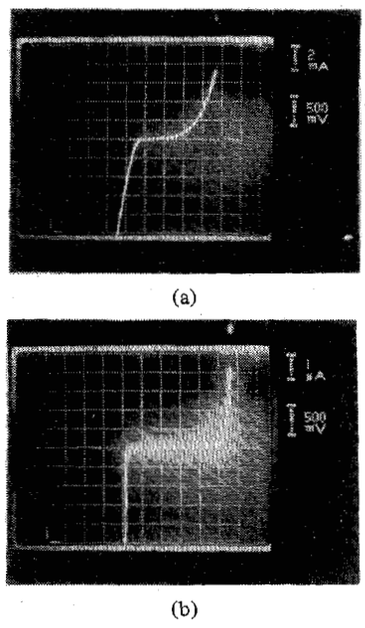

Fig. 2. Current-voltage characteristics in the substrate circuit. Source and drain are grounded; the total area of alloyed contacts is 3×10^{-5} cm^2. (a) $T = 300$ K; (b) $T = 77$ K.

As discussed in [1], The NERFET can exhibit NDR in two distinct configurations, depending on a circuit connection of the substrate terminal. In the floating-substrate arrangement the hot-electron injection induces charge in the substrate and thus shifts the threshold for conduction in the main channel. This process is limited by thermionic injection of cold electrons from the substrate whose potential is raised by the injected charge. For a barrier height $\psi = 0.4$ eV, we can expect a pronounced NDR in this mode only at low temperatures. Fig. 3(a) shows the observed current-voltage (I_D-V_D) characteristics in the drain circuit. These characteristics were taken in a quasi-floating configuration in which the substrate was positively biased through a large resistance, drawing a small constant current I_{SUB} (four orders of magnitude lower than that in the drain circuit). The four curves in Fig. 3(a) correspond to the gate voltage V_G varying from -0.2 to $+0.4$ V. We see that higher V_G suppresses the NDR in accordance with the theoretical predictions [1]. We also see a pronounced hysteresis in the I_D-V_D characteristics, which indicates a memory effect. This means that electrons transferred into the second conducting layer remain there when the drain voltage is reduced. The transferred electrons are free to move within the heavily doped second conducting layer, i.e., they are not localized on any traps. In the absence of I_{SUB}, the retention time is determined by the reverse thermionic emission of "cold" electrons from the substrate, which at low temperatures is a slow process. Introduction of a substrate leakage reduces the memory effect and at higher I_{SUB} the latter is no longer observed (Fig. 3(b)). Characteristics obtained at 4.2 K were quite similar to those at 77 K, which is another evidence that trapping effects in the AlGaAs barrier region are not important.

When both the substrate and the gate are floating, the device shows symmetric characteristics on a curve tracer.

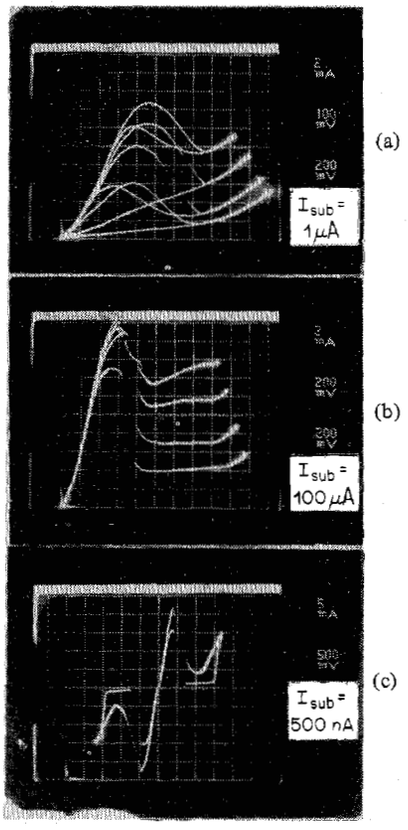

Fig. 3. Current-voltage characteristics in the drain circuit: floating-substrate configuration; $T = 77$ K. (a) $I_{SUB} = 1$ μA; $V_G = -0.2$, 0, 0.2, 0.4 V; (b) $I_{SUB} = 100$ μA; $V_G = -0.2$, 0, 0.2, 0.4 V; (c) $I_{SUB} = 0.5$ μA; floating gate.

Fig. 3(c) displays such curves with the peak-to-valley ratio in current reaching about 30. These characteristics were taken with the substrate current, $I_{SUB} = 500$ nA, being four orders of magnitude lower than the drain current.

Biased-substrate characteristics of the NERFET are shown in Fig. 4. We see a strong dependence of NDR on the substrate voltage V_{SUB}. It should be noted that the NDR portion of these curves represents an average over high-frequency oscillations, and its shape can be affected by parasitic impedances introduced by an experimental setup. The rising portion of I-V curves at high V_D corresponds to the onset of the thermionic emission of cold electrons from the substrate into the drain. It is shifted to the right by increasing V_{SUB}. The observed strong effect of V_{SUB} on the depth of NDR is, in our view, related to the dynamical charge storage effect discussed in [1]. Hot electrons emitted over the top of the barrier drift downhill with a saturated velocity v_s, and constitute a space charge of volume density $\rho = J/v_s \equiv \Delta\sigma/l$, where J is the substrate current density and $\Delta\sigma$ the surface density of charge stored in transit on the barrier of thickness l. For an efficient depletion of the channel one must have $\Delta\sigma \sim I/v_s$, where $I \sim 2$ to 3 A/cm is the peak channel current per unit gate width, cf., Fig. 4. Assuming that the saturated velocities are $\sim 10^7$ cm/s both in the channel and on the barrier, we find $\Delta\sigma \approx 2 \times 10^{12}$ e/cm^2. This corresponds to a space-charge potential $\Delta\psi = \rho l^2/2\epsilon \approx 2$ V. In order to overcome this additional barrier, the substrate bias V_{SUB} must exceed

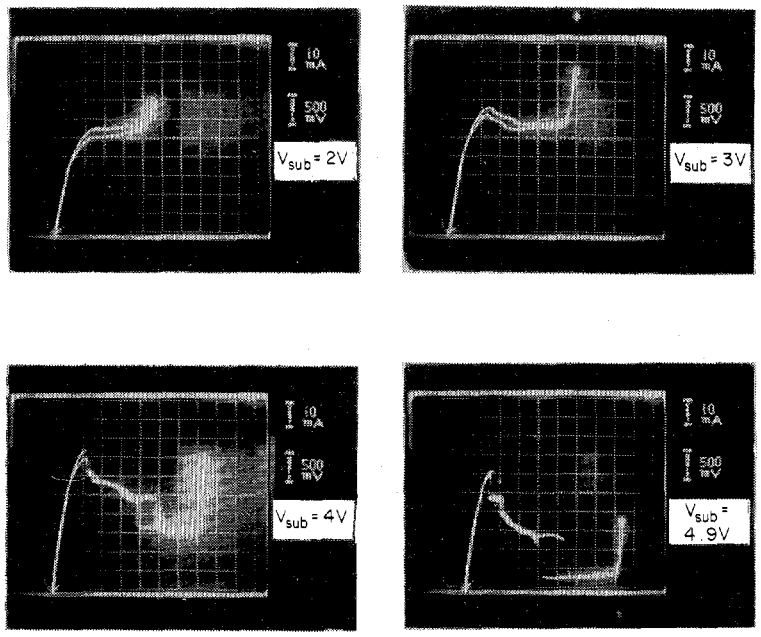

Fig. 4. Current–voltage characteristics in the drain circuit: biased-substrate configuration; $T = 77$ K; $V_G = 0$.

$\Delta\psi$. Thus for the indicated current densities in the biased-substrate configuration the NDR is obtained only when $V_{SUB} \gtrsim 2$ V, see Fig. 4.

We remark that dynamical charge storage due to space-charge-limited current is an important factor in most unipolar devices. In these devices the injected charge screens the applied field and limits the efficiency of injection (for a detailed discussion of charge injection in field-effect and analog transistors see [3], [4]). Unlike in any other device with space-charge-limited current, in NERFET this current flows perpendicular to the main conducting channel and results in the desired effect of channel depletion and NDR. It is interesting to note that the decrease in I_D in the NDR region does not necessarily imply a simultaneous increase in I_{SUB}. Moreover, the first appearance of the NDR is, in fact, accompanied by a small drop in the substrate current. We believe this effect is associated with the formation of a narrow high-field domain in the channel in the vicinity of the drain. Concentration of the electron field enhances hot-electron injection. On the other hand, concentration of the substrate current in a narrow strip ("hot filament", extending over the 250 μm of gate width) results in a higher density of the dynamically stored charge and further depletion of the channel. In this process, the increasing density J of the substrate current does not necessarily imply higher I_{SUB}.

Dimensions of the hot filament can be estimated from the continuity equation for the channel current $I(x)$ per unit gate width, $dI/dx = -J$, where x is the direction of the channel. Taking $I = \sigma v_s$ in the high-field domain and

$$J = \frac{\sigma}{\Delta}\sqrt{\frac{kT_e}{2\pi m}}\, e^{-e\psi/kT_e}$$

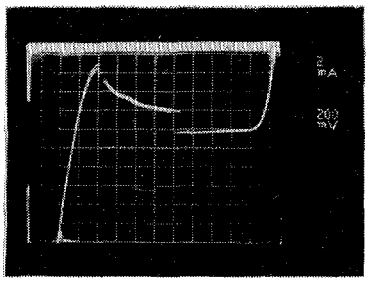

Fig. 5. NERFET at room temperature: biased-substrate configuration; $V_{SUB} = 2.4$ V; $V_G = 0.6$ V ($T = 300$ K).

where Δ is the channel thickness and T_e the electron temperature, we find that the density of charge in the high-field domain decays exponentially from the beginning of the domain and toward the drain with a characteristic length $\lambda = \Delta v_s(kT_e/2\pi m)^{-1/2} \exp(e\psi/kT_e)$. The effective extent of the hot filament is, thus determined by the electron temperature, and at high T_e it may be narrower than the high-field domain.

The dynamical charge storage effect can be expected to have only a weak dependence on the lattice temperature (mainly through the dependence $T_e(T)$ in the high-field domain). Fig. 5 shows the observed characteristics at $T = 300$ K in the biased-substrate configuration. Dependence of the room temperature characteristics on V_{SUB} and V_G was qualitatively similar to that at 77 K. In particular, the substrate works as a backgate, i.e., positive V_{SUB} enhances the density of charge in the channel and therefore the peak value of the drain current.

We never observed an NDR effect at 300 K in the floating-substrate configuration. This underscores the difference in the physical principles involved in the operation of NERFET in

these two circuit configurations: static versus dynamic charge storage. We believe that substrate-biased NERFET may become useful as an efficient generator of microwaves in the millimeter-wave region, controllable by the gate and substrate voltages. Of particular importance is the complete absence of memory effects in the dynamic mechanism. In a recent work [5] we observed the microwave generation in NERFET in the gigahertz range. It is experimentally demonstrated in [5] that the NDR and the associated instabilities are not related to spurious oscillations often observed in transistors with poor isolation. Estimates show [6] that the intrinsic speed of operation in NERFET is limited by the energy relaxation time and the time of flight of electrons over the graded barrier, both of these delays being of order several picoseconds.

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