Lateral interband tunneling transistor in silicon-on-insulator

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We report on a lateral interband tunneling transistor, where the source and drain form a heavily doped lateral *pn* junction in a thin Si film on a silicon-on-insulator (SOI) substrate. The transistor action results from the control of the reverse-bias tunneling breakdown under drain bias V_D by a gate voltage V_G. We observe gate control over tunneling drain current I_D at both polarities of V_G with negligible gate leakage. Systematic $I_D(V_G,V_D)$ measurements, together with numerical device simulations, show that in first approximation I_D depends on the maximum junction electric field $F_{\max}(V_G,V_D)$. Excellent performance is hence predicted in devices with more abrupt junctions and thinner SOI films. The device does not have an inversion channel and is not subject to scaling rules of standard Si transistors. © *2004 American Institute of Physics.* [DOI: 10.1063/1.1668321]

The interest in quantum semiconductor tunneling structures dates back to the Esaki tunnel diode.[1] In the early days, the sharply nonlinear current–voltage $I(V)$ relation of a two-terminal device gave rise to a variety of circuit ideas,[2] but these hopes were swept away by the rapid evolution of transistors with their decisive advantage of a three-terminal operation with input–output isolation. A number of tunneling devices have been demonstrated in III–V heterostructures over the past two decades, but useful circuit functionality has proved elusive.[3] Furthermore, the integration of tunneling-based III–V heterostructures with the dominant Si complementary metal-oxide-semiconductor (CMOS) technology is difficult. The attention has therefore turned to Si-based tunneling devices that may enhance some critical functions (logic, speed) without impacting main CMOS transistors.[4] Fully depleted silicon-on-insulator (SOI) transistors are predicted[4,5] to take over from bulk Si CMOS devices in the near future. In the context of this development, the ultrathin Si films available in SOI technology[6] have opened new avenues for CMOS-compatible tunneling devices. In this letter, we report on the lateral interband tunneling transistors (LITT) based on gate-controlled source-drain tunneling in a heavily doped lateral *pn* junction in a thin Si film on SOI, fully compatible with standard CMOS devices and processing.

Three-terminal surface controlled source-breakdown structures were originally proposed by Shockley and Hopper[7] in the context of a *pn* avalanche process and later studied by Quinn and co-workers to understand the physics of a quasi-two-dimensional electron channel.[8] The first successful efforts to fabricate such field-effect-transistor (FET)-like interband tunneling devices were made in III–V (mesa-type and planar p^+-i-n^+),[9] and in Si (planar p^+-p-n^+),[10] with p^+-drain and n^+-source doping. These studies demonstrated gate-controlled negative differential resistance, with V_G controlling the electric field F between the inversion n channel and the p^+- drain. The effective cross-sectional area of the channel-drain *pn* junction was kept small by the physical depth of the inversion channel. A similar device was also realized in a Si, vertical p^+-i-n^+ structure, gated on the sidewall, showing a FET-like quasisaturation of the drain current at relatively high gate voltages $V_G > 10$ V.[11] However, all of these FET-like devices employ an inversion channel, which increases the device area and adds gate capacitance, without performing any active function (since it is the tunneling resistance at the channel-drain junction, rather than the resistance of the channel itself, that determines I_D).

The difficulty in designing a three-terminal interband tunneling device in a field effect geometry is to obtain a sharp *pn* junction with sufficient doping for tunneling to take place without producing a large-area *pn* junction region underneath that would add leakage and capacitance. Our approach in LITT devices[12] starts directly with a heavily doped lateral *pn* junction in a thin Si film (shown in Fig. 1). The thin Si film reduces the source-drain capacitance and leakage current, while V_G (of either polarity) alters the maximum electric field $F_{\max}$ by adding a vertical field component to the V_D-controlled lateral field in the junction. Both forward and reverse source-drain bias operation are possible. Reverse-bias $V_D < 0$ favors high-speed applications due to the absence of minority carrier injection. In principle, a very short gate ($L_G \sim 10$ nm) could overlap the depletion region only, which would minimize gate capacitance and device area (dictated by the source and drain contacting requirements). While the possibility of such ultrashort gate lengths has al-

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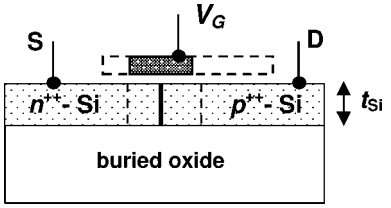

FIG. 1. Schematic layout of a LITT implemented in SOI, bold line marks the *pn* junction while the dashed lines indicate the corresponding lateral depletion region. In the ideal LITT, the gate overlaps the depletion region only to minimize capacitance (hatched); in our first fabricated prototypes, the gate overlaps the source and drain regions (dashed).

ready been demonstrated,[13] our proof-of-concept prototypes were fabricated in a standard optical-lithography SOI process modified by a double implantation sequence for the source-drain *pn* junction. We began with standard Unibond SOI substrates with 400 nm buried oxide (BOX) and 200 nm Si film on top of BOX. After thinning the SOI Si film to 40–50 nm thickness, the entire active area was doped p^+ by boron implantation (in the $2-6\times10^{19}$ cm^{-3} range) and annealed to activate the B implant. Then, half the active area was covered using a shifted active area mask level and the exposed source region was implanted n^{++} with phosphorus, aiming for $n^{++}\sim10^{20}$ cm^{-3} net effective doping (doping levels were estimated by process simulation[14]). Subsequent processing followed the standard SOI CMOS sequence with 4 nm deposited gate oxide, n^+-poly Si gate, and optical lithography for gate definition. Relatively wide gate lengths $L_G=0.35-0.5\ \mu$m were employed to ensure the overlap between the gate and the *pn* junction simultaneously resulting in a significant overlap between the gate and the source/drain regions (Fig. 1).

The room-temperature $I_D(V_G,V_D)$ characteristics of reverse-biased ($V_D<0$) LITT devices with ~40 nm film thickness are shown in Fig. 2(a) for $|V_G|\leqslant5$ V. At $|V_G|>3$ V a source-drain current I_D begins to flow at moderate drain bias $V_D=-1$ V. This drain current is largely independent of L_G. No measurable gate leakage is observed for $|V_G|\leqslant5$ V. Given the heavy *pn* junction doping, I_D certainly

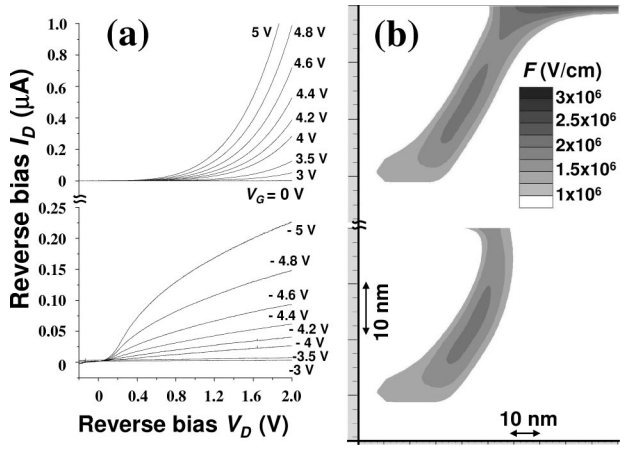

FIG. 2. (a) Reverse-bias $I_D(V_D,V_G)$ curves for LITT with *pn* junction doping of $6\times10^{19}-10^{20}$ cm^{-3} at $T=300$ K as a function of V_G (device parameters: gate length $L_G=0.35\ \mu$m, width $W=10\ \mu$m, Si film thickness $t_{Si}\sim40$ nm, gate oxide ~5 nm); (b) Simulations of the spatial variation of F in the device for $V_G=2$ V (upper) and $V_G=-2$ V (lower), both at $V_D=-1$ V.

arises from carriers tunneling across the narrow depletion region, with V_G providing the additional vertical field contribution to F_{max}. As expected, both polarities of V_G promote tunneling I_D, but the effect is not symmetric with respect to polarity. While in our devices the asymmetry is due primarily to the unequal doping, the asymmetry would persist even if the *pn* structure were perfectly symmetric. Indeed, the application of $V_G>0$ promotes the tunneling process with a final state where a hot electron slides downhill in the conduction band. In contrast, $V_G<0$ produces hot holes floating up the valence band.

As seen in Fig. 2, the turn-on V_G values are rather large, indicating that the built-in lateral electric field F is small due to insufficient junction doping abruptness. This explanation is consistent with the doping split dependence of the LITT characteristics: identically processed devices with lower doping on the p side exhibited less tunneling current.[12] Furthermore, at $V_G=0$, when the junction field F is almost entirely due to V_D, large reverse drain voltages~-3 V are required before I_D begins to flow, again confirming insufficient junction doping.

A fundamental difficulty of inserting Si-based interband tunneling devices into future Si circuitry arises from the lack of reliable physical models of interband tunneling in indirect band-gap materials. In Si, the hole states at the top of the valence band lie near the center (Γ point) of the Brillouin zone (BZ), while electron states at the bottom of the conduction band are displaced by roughly three-fourths of BZ in the $\langle100\rangle$ X point direction. Thus, tunneling from the valence to the conduction band requires momentum transfer from either phonons or impurities. Various numerical approaches extending the work of Keldysh[15] and Kane and Blount[16] for indirect interband tunneling obtained expressions with adjustable electron-phonon coupling parameters.[17,18] Although these expressions (also used by all industrial device simulators) are of questionable predictive value, their consistent outcome is a strong exponential-type dependence of the tunneling current on the maximum electric field F_{max} in the junction. Given the device geometry of Fig. 1, the spatial variation of $F_{max}(V_G,V_D)$ is complex, with V_G accumulating one side of the junction and depleting the other. As a result, the dependence of F_{max} and hence I_D on V_G polarity is asymmetric because of the differences in the doping level (n^{++} source more heavily doped than p^+ drain) and the work function difference between the n^+-poly-Si gate and the drain. This asymmetry is observed in the $I_D(V_G,V_D)$ data of Fig. 2(a) as well as in the two dimensional (2D) simulation of $|F|$ for $V_G=\pm2$ V and $V_D=-1$ V across the junction in Fig. 2(b).

In order to gauge the potential improvements of our device performance as a function of junction parameters, we simulated $F_{max}(V_G,V_D)$, using both our real devices (simulated using the actual double-implantation process parameters) and ideal devices with abrupt *pn* junctions. The comparison between the "real" and abrupt junction devices explains the large $|V_G|>3$ V values required to turn on tunneling in Fig. 2(a) and points to possible performance improvements, including low gate and drain bias operation at ~1 V, in compliance with scaled CMOS circuitry. Figure 3(a) shows a comparison of simulated $F_{max}(V_G,V_D=-1\text{ V})$, for our real double-implanted prototype and a de-

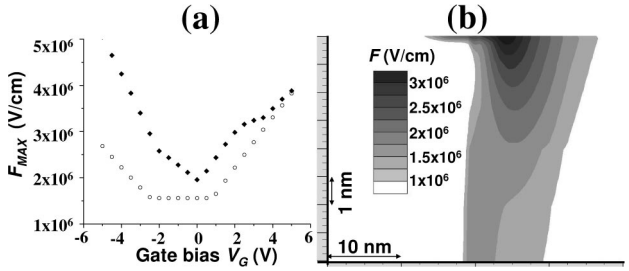

FIG. 3. (a) Simulated maximum electric field F_{MAX} vs V_G at $V_D=-1$ V in the fabricated double-implanted prototype devices (circles) and a hypothetical optimized device with a perfectly abrupt *pn* 1.5×10^{19}–4.5×10^{19} junction, thinner silicon film $t_{\mathrm{Si}}=8$ nm, $L_G=9$ nm, and 2 nm gate oxide (diamonds); (b) spatial variation of F in the optimized device for $V_G=2$ V at $V_D=-1$ V, note the higher F_{MAX} compared to Fig. 2(b).

vice with an ideally abrupt 1.5×10^{19}–4.5×10^{19} cm^{-3} *pn* junction in a thinner Si film with an ultrashort L_G. As also shown by the 2D cross-sectional spatial F plot of the abrupt junction device in Fig. 3(b), abrupt *pn* junctions in a thinner film produce much higher $F_{\max}$ values, promising operation at lower gate bias $|V_G|\sim1$ V. Here it should be noted that the functionality of ultrathin SOI ($t_{\mathrm{Si}}<10$ nm) has already been demonstrated for MOSFET[19–21] and tunneling transistor[22] applications. The asymmetry of $F_{\max}$ about $V_G=0$ in Fig. 3(a) can be largely avoided using a midgap gate material with a symmetric work function with respect to the *p* and *n* sides of the junction, or by an intentionally asymmetric *pn* doping profile as in the optimized device of Fig. 3(b).

Unlike a normal MOSFET, the LITT has no obvious current saturation mechanism: I_D should increase with both V_D and V_G, limited only by extrinsic factors, such as series resistance in the contacts. If we consider a LITT operated in reverse bias for high-speed analog amplification, the limitation on its high-frequency operation arises essentially from the capacitance, since there is no minority carrier storage. However, given the absence of the inversion channel, the gate capacitance in the ideal LITT of Fig. 1, where a narrow gate overlaps the source-drain depletion only, is minimal. As for the source-drain capacitance, it depends on the doping level of the *pn* junction. True Esaki diodes, with highly degenerate doping on both sides of the junction, have good high-speed response even in forward bias.[23] In the LITT, the tradeoff between source-drain capacitance (increasing with *pn* junction doping) and the tunnel resistance (decreasing with *pn* junction doping) will determine the proper design point.

It should be emphasized that the double implantation procedure employed to produce our prototype LITT devices is far from ideal, with the source region undergoing two high-dose implantations and the junction sharpness suffering from lateral diffusion during activation. Epitaxial regrowth of the n^+-Si source region may be a solution. Masking half the active area with SiO_2, removing nearly all the p^+-Si (leaving a thin ~1 nm layer above the BOX, which would be depleted for all operating V_G and V_D) and regrowing selectively n^{++} Si, it may be possible to realize an abrupt lateral junction at the cost of a nonplanar step. The gate would then be aligned to this step. Like many other innovative SOI concepts, the LITT still awaits an optimized process. Finally, we note that with source and drain contacts of opposite polarity, the LITT is not affected by short channel effects and does not obey the scaling limitations of a MOSFET, at least not in any obvious way. This may become critical for future end-of-the-roadmap ULSI devices.

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