Generation of Equivalent Circuits from Physics-Based Device Simulation

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***Abstract*—A novel technique for the numerical extraction of equivalent circuits from physics-based device simulation is presented. The method is based on the partitioning of the device into functional regions, each corresponding to a circuit block. All the circuit elements have a clear physical interpretation. Element values are directly obtained from small-signal dc device simulation. The method generates equivalent circuits of a complexity similar to the traditional approach, with model generation times comparable with those of black-box and physics-based device models. Applications to one-dimensional pn junctions and bipolar transistors are presented, discussing the extraction algorithm in detail.**

***Index Terms*—Circuit, device models, modeling, simulation.**

I. Introduction

DEVICE modeling for circuit applications faces conflicting requirements of accuracy, efficiency, and development time. In the common approach to device modeling, idealized analytical expressions are fitted to extensive measurements [1]. Such models offer good efficiency and accuracy in their range of validity. However, analytical models show limitations when applied to highly nonideal devices. In such cases, either the existing models are forcibly adapted to the measured data, thus losing physical meaning, or new models must be developed. Black-box and table-based approaches seek to alleviate this problem by fitting purely numerical models to experimental data [2]–[7]. Short development times and good accuracy may be achieved, at the cost of a loss of physical meaning of the model parameters. Finally, physics-based device simulation achieves satisfactory accuracy in a short development time, but the associated computational cost prevents its application to circuits comprising more than a few devices [8], [9].

In this paper, we investigate a fourth alternative, consisting in the direct, automatic extraction of equivalent circuits from device simulations [10], [11]. The circuit topology and elements have a direct interpretation in terms of device physics. Also, the number of elements is comparable with a traditional model. On the other hand, the model generation time is similar to that of physics-based simulation. The accuracy that can be achieved with this technique largely depends on the validity of the assumptions made when reducing continuous functions, as obtained from the physical device simulation, to a small set of lumped elements. We will show that in a number of realistic cases, excellent high-frequency device models are obtained.

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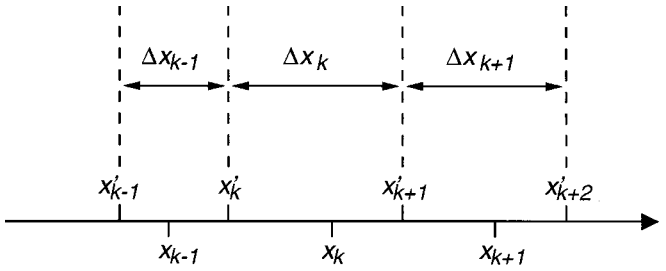

Fig. 1. Discretization mesh in one dimension, showing the points x_k and the domains (boxes) Δx_k.

The work proceeds as follows. In Section II, the equivalent circuit topology is rigorously derived from integral formulations of the Poisson and continuity equations in one dimension. In Section III, the branch-constitutive equations for the various circuit elements, i.e., the expressions of charges and currents as functions of the internal voltages, are discussed. In Section IV, the extraction of element values from device simulations is described. Section V presents examples of equivalent circuit generation for pn junction diodes and bipolar transistors. Conclusions are drawn in Section VI.

II. Kirchhoff Current Equations

The rigorous derivation of circuit equations from the Poisson and continuity equations was first made by Sah [12], based on a previous treatment by Linvill [13]. However, the original formulation holds only in the ideal limit of a very small semiconductor region, and for linear transport. A "lumped" formulation for regions of finite size was also proposed, based on finite differences [12], [14], [15]. However, due to discretization errors, accurate solutions are obtained with this method only if the device is partitioned into a large number of small regions [16]. We have generalized the approach by allowing regions of arbitrary size, by use of box integration [17] instead of finite differences. The procedure is described here in a one-dimensional (1-D) case, but extension to higher dimensionality is straightforward. Let us assume on the x axis a discretization mesh (Fig. 1) as defined by the $n+1$ points $x_0 \ldots x_n$. Around each point x_k, we define a domain (box) Δx_k as the region included between two points x'_k and x'_{k+1}. The points x'_k are arbitrarily positioned, with the only constraint that $x_{k-1} < x'_k < x_k$. The total hole and electron charges stored in the domain Δx_k are defined as

$$Q_p^k = e \int_{x'_k}^{x'_{k+1}} dy\, p(y) \tag{1}$$

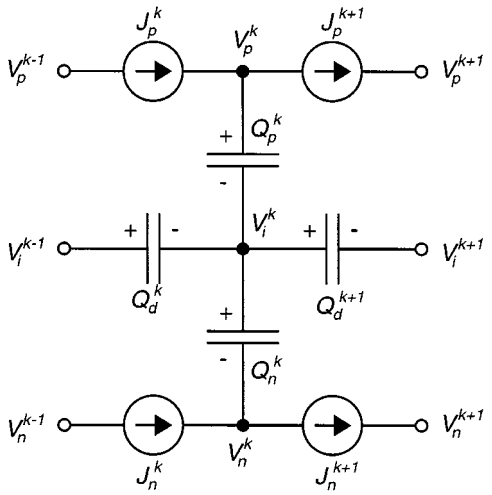

Fig. 2. Equivalent circuit representation of the Poisson and continuity equations. Capacitors Q_d^k, Q_p^k, and Q_n^k represent the displacement-vector, hole, and electron terms entering the Poisson equation, respectively. Current sources J_p^k and J_n^k represent the hole and electron conduction currents.

$$Q_n^k = e\int_{x_k'}^{x_{k+1}'} dy\, n(y). \tag{2}$$

Likewise, the hole, electron, and displacement currents at each boundary x_k' are defined as

$$J_p^k = J_p(x_k') \tag{3}$$
$$J_n^k = J_n(x_k') \tag{4}$$
$$J_d^k = \epsilon(x_k')\frac{d}{dt}E(x_k') \tag{5}$$

where $J_p(x)$ and $J_n(x)$ are the (space-dependent) hole and electron current densities, $J_d(x)$ is the displacement current, $\epsilon(x)$ is the dielectric constant, and $E(x)$ is the electric field. By straightforward integration of the Poisson and continuity equations, one then obtains

$$\frac{d}{dt}Q_p^k - \frac{d}{dt}Q_n^k = J_d^{k+1} - J_d^k \tag{6}$$
$$\frac{d}{dt}Q_p^k = J_p^k - J_p^{k+1} \tag{7}$$
$$\frac{d}{dt}Q_n^k = J_n^{k+1} - J_n^k. \tag{8}$$

Equations (6)–(8) can be recognized as the Kirchhoff current equations for the circuit of Fig. 2. The three node voltages are defined as

$$V_i^k = \phi_i(x_k)$$
$$V_p^k = \phi_p(x_k)$$
$$V_n^k = \phi_n(x_k)$$

where ϕ_i is the intrinsic (electrostatic) potential, and ϕ_p and ϕ_n are the hole and electron quasi-Fermi potentials. By analogy with the hole and electron currents, the displacement current J_d^k may also be seen as flowing through a "capacitor" whose stored charge is

$$Q_d^k = \epsilon(x_k')E(x_k') \tag{9}$$

thus, allowing a uniform circuit representation of the Poisson equation. Note that in the limit of vanishing space regions, the above formulation reduces to the model originally presented by Sah [12].

III. Branch-Constitutive Equations

In Section II, internal device quantities (charge and current) have been lumped into discrete terms by space integration, in order to derive a circuit topology. The above derivation did not involve any approximation. However, the definition of a practical circuit also requires *branch-constitutive equations* for each element, i.e., relations between the node voltages and the branch currents (or charges in the case of capacitors). In the drift-diffusion approximation, the charges in (1) and (2) and currents in (3)–(5) can be written in terms of the three potentials $\phi_i(x), \phi_p(x)$, and $\phi_n(x)$ and their space derivatives. The calculation of the charges and currents from these equations, then, requires knowledge of the three potential distributions over the entire device. Such a formulation is not well suited to a compact circuit model, which should have a limited number of discrete state variables. In the following, we will seek an approximate representation which can still describe the physical behavior of each device region with good accuracy. In particular, we will assume all currents and charges to be functions of the discrete voltages V_i^k, V_p^k, and V_n^k at the mesh nodes x_k, rather than being functionals of the continuous potential distributions.

First of all, it is reasonable to make a *local quasi-static approximation* and assume that all the charges depend on voltages at the local node

$$Q_d^k \approx f_d^k\left(V_i^{k-1} - V_i^k\right) \tag{10}$$
$$Q_p^k \approx f_p^k\left(V_p^k - V_i^k\right) \tag{11}$$
$$Q_n^k \approx f_n^k\left(V_i^k - V_n^k\right). \tag{12}$$

The above equations are derived by analogy with the familiar expression for the electric field, and the Boltzmann statistics

$$E = -\frac{d}{dx}\phi_i \tag{13}$$
$$p = n_i \exp[e(\phi_p - \phi_i)/kT] \tag{14}$$
$$n = n_i \exp[e(\phi_i - \phi_n)/kT]. \tag{15}$$

We note that in the context of device modeling, the quasi-static approximation usually assumes the dependence of internal charge on the device terminal voltages, i.e., the *external* voltage nodes. A *local* quasi-static approximation, on the other hand, assumes the dependence on the charge on a single *internal* circuit node. Therefore, a local quasi-static device model with internal circuit nodes will be able to represent non-quasi-static effects.

Taking derivatives, we can now define a *dielectric capacitance*

$$C_d^k = \frac{dQ_d^k}{d\left(V_i^{k-1} - V_i^k\right)} \tag{16}$$

and electron and hole *charge-storage capacitances* at each node

$$C_p^k = \frac{dQ_p^k}{d\left(V_p^k - V_i^k\right)} \tag{17}$$

$$C_n^k = \frac{dQ_n^k}{d\left(V_i^k - V_n^k\right)}. \tag{18}$$

The integral Poisson equation (6), combined with the definitions (16)–(18), now reads as follows:

$$\begin{aligned} &C_p^k\left(v_p^k - v_i^k\right) - C_n^k\left(v_i^k - v_n^k\right) \\ &\quad = C_d^{k+1}\left(v_i^k - v_i^{k+1}\right) - C_d^k\left(v_i^{k-1} - v_i^k\right) \end{aligned} \tag{19}$$

where lowercase symbols denote small-signal voltages. (In the derivation of (19), the time derivative has been omitted, assuming that the small signals have zero dc values.) Equation (19) is the Kirchhoff current equation for the middle node in the circuit of Fig. 2. The small-signal current equations for the remaining two nodes are obtained from (7)–(8) as

$$C_p^k\left(\frac{d}{dt}v_p^k - \frac{d}{dt}v_i^k\right) = j_p^k - j_p^{k+1} \tag{20}$$

$$C_n^k\left(\frac{d}{dt}v_i^k - \frac{d}{dt}v_n^k\right) = j_n^{k+1} - j_n^k. \tag{21}$$

In order to derive the branch-constitutive equations for the current sources in the circuit of Fig. 2, we can also start from the microscopic current equations

$$J_p = -e\mu_p p\nabla\phi_p$$
$$J_n = -e\mu_n n\nabla\phi_n.$$

Differentiating the above equations and rearranging, we obtain three terms

$$dJ_p = J_p(d\mu_p/\mu_p + dp/p + d\nabla\phi_p/\nabla\phi_p) \tag{22}$$

$$dJ_n = J_n(d\mu_n/\mu_n + dn/n + d\nabla\phi_n/\nabla\phi_n). \tag{23}$$

By analogy, we shall write the macroscopic currents as the product of three generic functions, corresponding to the relative variations of the carrier mobility, density, and Fermi "voltage", denoted by the subscripts m, d, and v, respectively

$$\begin{aligned} J_p^k &= eg_{mp}^k\left(V_i^{k-1} - V_i^k\right) \\ &\quad \times g_{dp}^k\left(V_p^{k-1} - V_i^{k-1}, V_p^k - V_i^k\right) \\ &\quad \times g_{vp}^k\left(V_p^{k-1} - V_p^k\right) \end{aligned} \tag{24}$$

$$\begin{aligned} J_n^k &= eg_{mn}^k\left(V_i^{k-1} - V_i^k\right) \\ &\quad \times g_{dn}^k\left(V_i^{k-1} - V_n^{k-1}, V_i^k - V_n^k\right) \\ &\quad \times g_{vn}^k\left(V_n^{k-1} - V_n^k\right). \end{aligned} \tag{25}$$

Note that in the above equations, the functions g_{dp}^k and g_{dn}^k play a role analogous to the carrier density in (22) and (23). However they may be numerically different from the stored hole and electron charges, which we have denoted as f_p^k and f_n^k. For generality, g_{dp}^k and g_{dn}^k are assumed to be driven by controlling voltages $V_p - V_i$ and $V_i - V_n$ at both left and right side of the region, i.e., at x_{k-1} and x_k. By taking derivatives, we obtain the small-signal currents as four separate controlled current sources

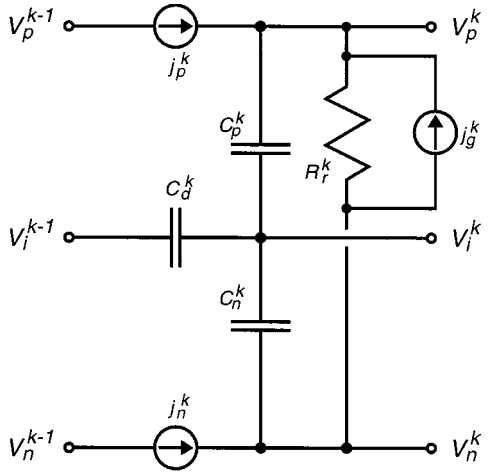

Fig. 3. Complete small-signal equivalent-circuit representation of the Poisson and continuity equations, including recombination.

$$\begin{aligned} j_p^k &= G_{mp}^k\left(v_i^{k-1} - v_i^k\right) + G_{fp}^k\left(v_p^{k-1} - v_i^{k-1}\right) \\ &\quad + G_{rp}^k\left(v_p^k - v_i^k\right) + G_{vp}^k\left(v_p^{k-1} - v_p^k\right) \end{aligned} \tag{26}$$

$$\begin{aligned} j_n^k &= G_{mn}^k\left(v_i^{k-1} - v_i^k\right) + G_{fn}^k\left(v_i^{k-1} - v_n^{k-1}\right) \\ &\quad + G_{rn}^k\left(v_i^k - v_n^k\right) + G_{vn}^k\left(v_n^{k-1} - v_n^k\right). \end{aligned} \tag{27}$$

The current sources $G_{fp}^k, G_{rp}^k, G_{fn}^k$, and G_{rn}^k correspond to the effect of the modulation of carrier density on the current density [terms dp/p and dn/n in (22) and (23)]. The subscripts f and r refer to the "forward" and "reverse" control of charge on current at nodes x_{k-1} and x_k. The generators G_{vp}^k and G_{vn}^k describe the effect of the variation of the quasi-Fermi level gradients on the current densities, and are in fact simple resistors [terms $d\nabla\phi_p/\nabla\phi_p$ and $d\nabla\phi_n/\nabla\phi_n$ in (22) and (23)]. Finally, the current sources G_{mp}^k and G_{mn}^k correspond to the change in current due to a change in the average electric field, due, e.g., to mobility modulation [terms $d\mu_p/\mu_p$ and $d\mu_n/\mu_n$ in (22) and (23)].

From a purely formal viewpoint, the four voltage-controlled current sources represent the linear dependence of the two currents j_n^k and j_p^k on the four boundary voltages $(v_p^{k-1}, v_p^k, v_i^{k-1}, v_i^k)$ for holes, $(v_i^{k-1}, v_i^k, v_n^{k-1}, v_n^k)$ for electrons. Note, however, that the four controlling voltages in (26)–(27) are not independent, since for example

$$\begin{aligned} &\left(v_i^{k-1} - v_i^k\right) + \left(v_p^{k-1} - v_i^{k-1}\right) \\ &\quad - \left(v_p^k - v_i^k\right) - \left(v_p^{k-1} - v_p^k\right) = 0. \end{aligned}$$

Therefore, only three linearly independent generators are needed in principle to describe the full small-signal current response of the system to a voltage input. For convenience, in the following we will maintain the notation with four conductances, keeping in mind that there is an infinity of choices for the four quantities that gives the same current response to a given voltage stimulus.

The full small-signal equivalent-circuit block for the semiconductor region $[x_{k-1}, x_k]$ is shown in Fig. 3. The complete schematics includes the capacitors and controlled generators

discussed above. Generation-recombination (G-R) is described to first order by a resistor R_r^k connecting the electron and hole quasi-Fermi levels v_n^k and v_p^k, so that the G-R rate is proportional to the energy difference between the two levels (i.e., the quantity $np - n_i^2$). This representation is exact for direct G-R, and also satisfactory if the trap occupancy can be assumed to be constant. If necessary, a rigorous trap-assisted G-R model can be obtained by introducing a separate circuit node for the trap occupancy [12]. External carrier generation (e.g., due to photon absorption) is likewise modeled by the current source j_g^k connecting the nodes v_n^k and v_p^k.

IV. Derivation of Circuit Elements from Device Simulation

In the ideal limit of a very fine discretization mesh (i.e., $\Delta x_k \to 0$ and $n \to \infty$), the approximations made in Section III become exact. Furthermore, in this case all the values of the circuit elements can be accurately derived from the microscopic charge and current equations, such as (13)–(15) and (22) and (23). For the realistic case of regions of finite size, no analytical approximation can satisfactorily model the dependence of the integral quantities (stored charges, electric fields) as a function of the voltages V_i^k, V_p^k, V_n^k. However, this information can be directly extracted from a device simulation. For example, the hole and electron charge storage capacitances can be computed as

$$C_p^k = \frac{\delta Q_p^k}{\delta\left(V_p^k - V_i^k\right)} \tag{28}$$

$$C_n^k = \frac{\delta Q_n^k}{\delta\left(V_i^k - V_n^k\right)} \tag{29}$$

where δ denotes small-signal differential quantities as obtained from a dc device simulation. Likewise, defining equations for the current-source conductances are found by rewriting (26)–(27), replacing small-signal currents and voltages by the corresponding values obtained from device simulation. Using the above definitions an equivalent circuit is obtained, which exactly duplicates the low-frequency behavior of the physical device simulation for the same applied small-signal voltage stimulus. Note that although only dc simulation results are employed, the model achieves ac predictive power by including charge-storage elements as capacitors. The small-signal solution can be obtained in two ways: 1) By direct subtraction of two solutions independently computed for bias points differing by a small voltage, e.g., 1 mV, or 2) By taking the real part of an ac solution at zero frequency [18]. The second method has the advantage of being free of the round-off error which is always present when very close numbers are subtracted.

The direct use of device simulation to compute element values sets the present treatment apart from techniques such as Linvill's Lumped Parameter approach [13], [19], [20] and Schilling's Regional Approximation Method [21]–[24] which rely on analytical formulations for each of the device regions. Our extraction technique can be directly extended to two- and three-dimensional (3-D) physical models of arbitrary complexity, including nonuniform doping profiles, hot-carrier and quantum-mechanical effects, as long as a small-signal dc solution is available from a numerical device simulator.

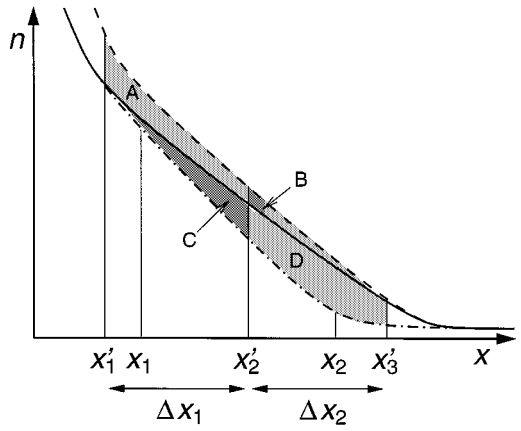

Fig. 4. Small-signal variations of the electron concentration in the base of an npn bipolar transistor. The base has been partitioned into two regions Δx_1 and Δx_2. The solid line represents the unperturbed concentration. The dashed and dot-dashed lines show the electron profile corresponding to an increase of base voltage and collector voltage, respectively. The total variations of stored charge in the domains Δx_1 and Δx_2 are shown as grey areas labeled A to D.

Equations (28)–(29) are directly applicable to two-terminal devices, where only one possible small-signal operation is possible. With three-terminal devices, a different set of circuit elements should in general be computed for each possible voltage stimulus. In the case of a bipolar transistor, one would obtain two different equivalent circuits, by grounding the collector and applying a small signal to the base, and vice versa. It is desirable, of course, to have a single circuit which satisfactorily describes the (possibly simultaneous) response to both terminal voltages. Since each of the current elements j_n^k and j_p^k is described by three degrees of freedom, it is possible in general to compute a set of conductances which exactly satisfy to up to three simultaneous, linearly independent constraints. Regarding capacitances, it is not possible, in general, to define values for C_d^k, C_p^k, and C_n^k which exactly satisfy to two different constraints. Let us consider for example the base region in an ideal npn bipolar transistor (Fig. 4). Two regions Δx_1 and Δx_2 are delimited by points (x_1', x_2') and (x_2', x_3') respectively. Two circuit nodes correspond to the physical points x_1 and x_2. When the base voltage is increased, the electron concentration increases mostly at the injection side (grey areas labeled A and B). On the other hand, when the collector voltage is modulated, the electron concentration stays approximately constant at the injection side, while it decreases at the collection side (areas C and D). The node x_1 is located on the injection side, so that the quantity $\delta(V_i^k - V_n^k) = (kT/e)\delta n(x_k)/n(x_k)$ is substantial for a base stimulus, and very small for the collector stimulus. On the other hand, the changes in the total charge for this node (areas A and C) are comparable for the two cases. Therefore the electron charge storage capacitance C_n^1 as computed by applying a small signal to the collector will be higher than if the same signal is applied to the base. A similar effect will be observed for the electron capacitance at point x_2 (areas B and D), but in this case the capacitance C_n^2 obtained from the base stimulus will be larger than that computed from the collector stimulus.

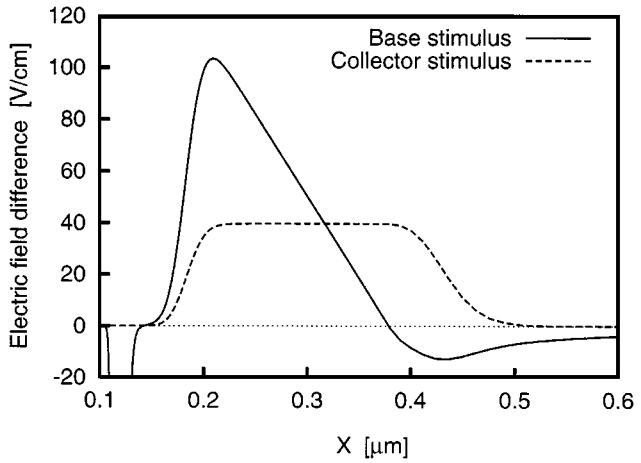

Fig. 5. Small signal variations of the electric field in a bipolar transistor, for a base stimulus (solid line) and a collector stimulus (dashed line). In both cases, the external voltage signal is 1 mV. The base-collector depletion region approximately extends between coordinates 0.2 μm and 0.4 μm.

An analogous remark applies to the electrostatic element C_d^k, computed by analogy with (16) as

$$C_d^k = \frac{\delta[\epsilon(x_k')E(x_k')]}{\delta\left(V_i^{k-1} - V_i^k\right)}. \tag{30}$$

In this case, it is possible that for small signals applied to two different terminals, the same change of the electrostatic potential drop between points x_{k-1} and x_k corresponds to different variations in the electric field at point x_k'. This will occur if the profile of the electrostatic potential is different, due for example to space-charge effects, as shown in Fig. 5 for the base-collector depletion region of a bipolar transistor. (Details of the simulated device are given in Section V.) The small-signal variation in the electric field is shown for a 1-mV voltage step applied to the base (solid line) and the collector (dashed line). The two stimuli have opposite polarity, in order to obtain the same change of the quantity $V_i^{k-1} - V_i^k$ (note that the integral of the two curves over the depletion region is the same). Let us assume a decrease in collector voltage and an increase of base voltage. In the former case, as the collector voltage is changed, the differential voltage is dropped uniformly across the depletion region. For a step in base voltage, instead, the electron current will increase. Due to velocity saturation, a uniform increase in the electron density will occur in the depletion region. The resulting uniform additional space charge is observed as the linear slope of the electric field profile. If the dielectric capacitance is computed from the base stimulus, its value strongly depends on the position of point x_k', and may be very different from the (well-defined) value obtained from the collector stimulus.

In principle, the problem of conflicting element definitions could be solved by replacing each pair of capacitors by a four-terminal charge element, defined by branch-constitutive equations such as

$$I_1 = C_{11}\frac{d}{dt}V_1 + C_{12}\frac{d}{dt}V_2$$
$$I_2 = C_{21}\frac{d}{dt}V_1 + C_{22}\frac{d}{dt}V_2.$$

With four available parameters C_{ij}, two constraints could be satisfied at the same time for each charge Q_i. This solution has two serious drawbacks: The total number of element values would double, obscuring the physical significance of the circuit; Furthermore, the presence of such nonreciprocal reactive elements could easily make the circuit unstable. Therefore, in the following we will retain the two-terminal capacitors, seeking heuristic arguments to optimize the accuracy of the approximate model.

Two possible approaches to the above problem can be pursued. One may think of defining each of the capacitors according to one or the other stimulus, according to the function the element plays in the overall circuit. For example, for best accuracy in the transconductance and diffusion capacitance, the base voltage only should be varied when computing element values in Fig. 4. An acceptable compromise would also be to modulate the base voltage to compute the capacitance at point x_1, while the collector voltage could be used for point x_2. Unfortunately, such considerations are not easily generalized, and require some *ad hoc* adjustments. A more general solution to the problem is obtained from the use of one of the following two expressions:

$$C_p^k = \frac{1}{2}\left(\frac{\delta_1 Q_p^k}{\delta_1\left(V_p^k - V_i^k\right)} + \frac{\delta_2 Q_p^k}{\delta_2\left(V_p^k - V_i^k\right)}\right) \tag{31}$$

$$\frac{1}{C_p^k} = \frac{1}{2}\left(\frac{\delta_1\left(V_p^k - V_i^k\right)}{\delta_1 Q_p^k} + \frac{\delta_2\left(V_p^k - V_i^k\right)}{\delta_2 Q_p^k}\right) \tag{32}$$

where δ_1 and δ_2 denote the two small-signal variations. Such formulations reduce to (28) if the two small-signal quantities are identical. If the stimuli are different, a ratio of sums is obtained, where the voltages (charges) are scaled in order to obtain identical differential charges (voltages). The same considerations apply to nonreciprocal effects in the dielectric capacitances.

As mentioned above, the current sources have more degrees of freedom than constraints. While this avoids any possible conflict, still one must supply the missing equations to determine all the circuit element values. In all cases, the symmetry constraint $G_{fp}^k = G_{rp}^k, G_{fn}^k = G_{rn}^k$ was empirically found to give the best results, thus reducing the degrees of freedom to two for two-terminal devices (single stimulus), and one for three-terminal (double stimulus). In the former case, the two needed equations have been derived from qualitative physical arguments. Different weights were assigned to the various current sources, according to the type of transport prevalent in the region, as estimated from the gradient of the quasi-Fermi levels and variations of carrier concentration. For three-terminal bipolar devices, one needs only one additional equation. For simplicity, it was assumed $G_{mp}^k = G_{mn}^k = 0$, as mobility modulation was not expected to play a significant role in the final circuit model.

V. Applications

The methodology described in the preceding sections has been implemented in a program for the fully automatic extraction of small-signal equivalent circuits for 1-D devices. Device simulation is employed to obtain the dc solution and the small-signal stimulus responses at a given bias point. Drift-diffusion solutions were obtained from the device simulator PADRE [25], however no special features of this simulator were used. Prior to circuit generation, the simulation region is

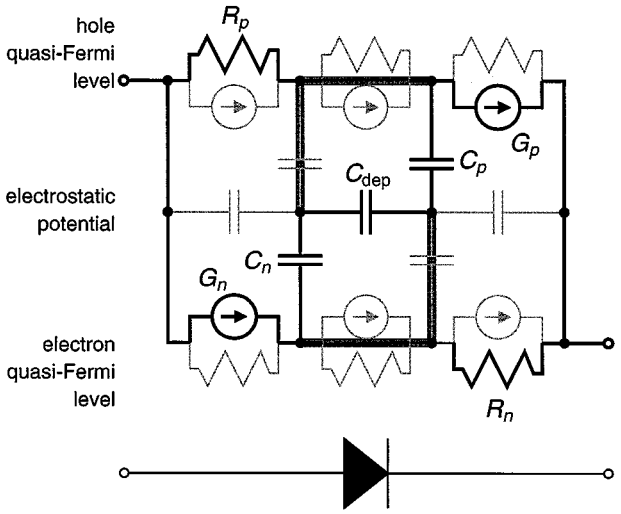

Fig. 6. Three-block equivalent circuit of a pn junction. The elements drawn in black are those which implement the minimum device functionality. The elements drawn in grey are only required for accurate high-injection and high-frequency modeling. The heavy dark lines highlight elements which reduce to short circuits in the low-injection case.

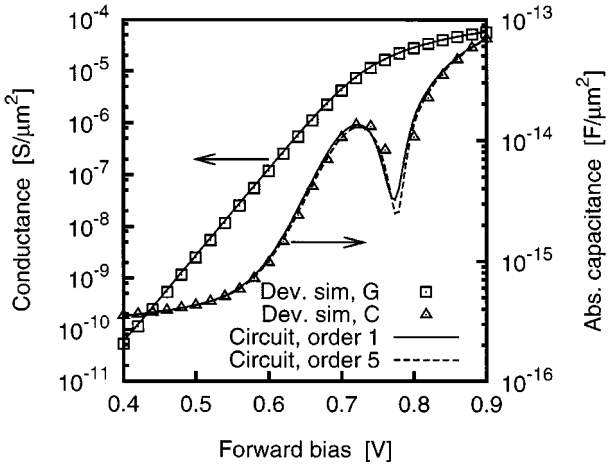

Fig. 7. Small-signal conductance and capacitance at 100 kHz for a symmetric pn junction with 5-μm-long p and n regions of doping 10^{16} cm^{-3}. The order parameter indicates the number of partitions chosen on each side of the junction. Symbols show device-simulation results. The dip in the capacitance corresponds to a change of sign at 0.77 V.

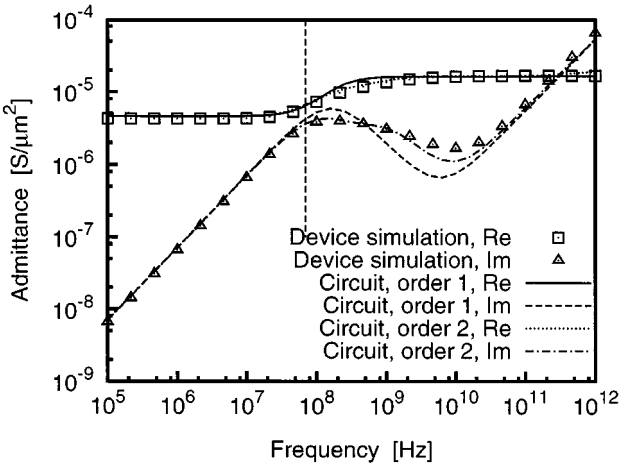

Fig. 8. Frequency response (real and imaginary part of the small-signal admittance) for the first- and second-order model of Fig. 7, at a forward bias of 0.7 V. The vertical dashed line indicates the diode cutoff frequency.

automatically divided into segments, based on the recognition of depletion regions and neutral regions. For each segment, one or more circuit blocks are generated. Usually a single block per region is sufficient. For very high frequency modeling, more than one block may be employed, e.g., to accurately compute the transmission-line effects in a quasi-neutral base. In most cases, the circuit extraction has been found to be robust with respect to the choice of partitioning, as long as sensible criteria are used. For example, one should preferentially place the nodes x_k at points where quantities do not display rapid (e.g., exponential) spatial variations, or else the energy levels at x_k will not properly represent the behavior of the surrounding region Δx_k.

The first example is an ideal pn junction, with uniform and symmetric doping of 10^{16} cm^{-3} in each of the 5-μm-long p and n regions. The mobility of electrons and holes is assumed constant and equal to 1000 cm^{2}V^{-1}s^{-1}. This simple reference device is similar to that presented in [26]. In this case, a minimum of three blocks are generated, one for each neutral region, and one for the depletion region. This minimal circuit is shown in Fig. 6, where the main elements are drawn in black (i.e., the minority carrier diffusion conductances and capacitances, depletion capacitance, and majority-carrier series resistance), while elements which are significant only for high-injection and high-frequency modeling are depicted in grey. The heavy dark lines highlight elements which reduce to short circuits in the low-injection case. Higher-order models are generated with more circuit blocks in the neutral regions. The depletion region is usually adequately described by a single block. Note that it is not necessary, in principle, to partition the device into regions according to physical criteria. One may locate the grid points x_k at arbitrary positions and still obtain a formally valid circuit. The positioning of grid points at the boundaries between regions of different physical properties, however, improves the accuracy of the method, and also endows the circuit elements with an immediate physical interpretation.

Fig. 7 shows the low-frequency conductance and capacitance as a function of applied voltage. The plot was obtained by computing a different equivalent circuit for each bias point, and obtaining the frequency response from ac circuit simulation. Note, however, that only the element values are function of the bias, while the topology is the same for all voltages. For high forward bias, the small-signal capacitance becomes negative, i.e., the device shows inductive behavior [26], [27]. As the two curves in Fig. 7 show, the use of multiple blocks in the n and p regions is not necessary for low-frequency modeling, as it improves the accuracy of the model only slightly. At high frequencies, however, the second-order model (with a total of five regions, two for each neutral region plus one for the depletion region) behaves substantially better than the first-order model (Fig. 8). The second-order model yields the correct frequency response well above the diode cutoff frequency. Note that while for Fig. 7 each data point corresponded to different element values, the result in Fig. 8 refers to a single model computed at a forward bias of 0.7 V.

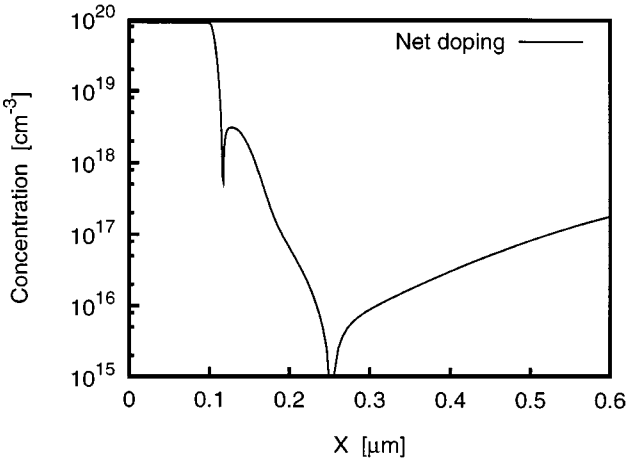

Fig. 9. Doping profile for a 0.25-μm npn bipolar transistor.

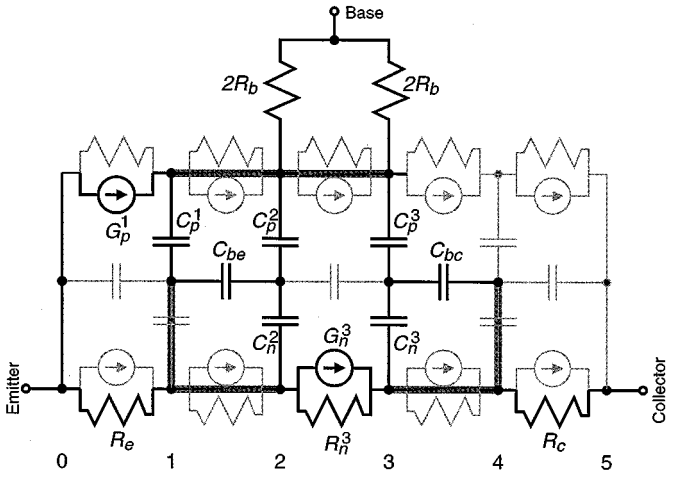

Fig. 10. Equivalent circuit of the npn bipolar transistor. The elements drawn in black are those which implement the minimum device functionality. The elements drawn in grey are only required for accurate high-injection and high-frequency modeling. The heavy dark lines highlight elements which reduce to short circuits at low injection.

As a second example, we show results for a bipolar transistor. The device parameters were obtained from a Lucent Technologies 0.25-μm BiCMOS process [28]. The device was assumed to be 1-D, therefore lateral effects (current spreading, extrinsic capacitances, etc.) were not accounted for. The metallurgical base length is 60 nm, with a graded base doping (Fig. 9). Although the simulated device was 1-D, a lumped base resistance of 1400 Ω was accounted for, both in the device and circuit simulation. We considered a base-emitter voltage of 0.9 V and collector-emitter voltage of 1 V, corresponding to a collector current of 430 μA/μm^2. In this bias condition, the simulated device displays a cutoff frequency f_T of 16 GHz (below the peak f_T) and $f_{\max}$ of 30 GHz. The device simulation employed a full physical model, including doping- and field-dependent mobility, trap-assisted and Auger recombination, and band-gap narrowing.

The extracted equivalent circuit is sketched in Fig. 10. For clarity, generation-recombination elements are not drawn. As in Fig. 6, only the main circuit elements are drawn in black, while elements which are important only for high-injection and high-frequency modeling are shown in grey. Resistors R_e and R_c represent the emitter and collector majority-carrier resistances. Capacitors $C_{\rm be}$ and $C_{\rm bc}$ are the depletion-layer capacitances, while C_p^1, C_n^2, and C_n^3 model minority charge storage in the emitter and base. Also important are capacitors C_p^2 and C_3^p, which represent the change in the Gummel number for a variation of emitter-base or collector-base voltage (such as the Early effect). Elements G_p^1, G_n^3, and R_n^3 represent the injection of minority carriers into the emitter and base. A lumped base resistance R_b is accounted for by an external circuit branch. All the other elements introduce nonidealities with respect to the basic model, for example the voltage drops in the emitter-base depletion layers, the dielectric capacitance of the neutral regions, etc.

In the case of the bipolar transistor, a double-stimulus extraction was performed. Small-signal solutions were obtained for steps of 1 mV both on base and the collector terminals. For this particular case, the best accuracy was obtained by extracting charge-storage and dielectric capacitances on the emitter side from the base stimulus, and those on the collector side from the collector stimulus. The reason for this choice can be understood from the circuit of Fig. 10. When a small voltage is applied to the collector, the current modulation (Early effect) is obtained as a partition of the collector voltage along two branches, namely, the electron quasi-Fermi levels (lower rail of the circuit), and the electrostatic potential (middle rail). While the definition of the generators in the electron-current branch is general enough to accommodate the responses to both base and collector stimuli, the charge-storage elements must be optimized for either one terminal response or another. Since the voltage partition is performed by capacitors C_p^3, C_n^3, and $C_{\rm bc}$, their values should be extracted from the collector stimulus.

Fig. 11 reports the frequency dependence of the common-emitter Y parameters. All the important low-frequency parameters are matched with good accuracy. Note how the error is limited to very high frequencies, above 100 GHz, and/or to second-order effects (e.g., the reverse trans-admittance Y_{12}). In all other cases, the error is of the order of 10%, and is due to the approximate expressions employed for the charge-storage and dielectric capacitances. This residual error could be eliminated by performing a further global optimization of the circuit, using the desired frequency response as a target. Since the needed adjustment is relatively small, convergence would be rapid. This final optimization step will in any case be necessary in order to compensate for the unavoidable discrepancies between the simulated device and the experimental measurements. Common causes of inaccuracy in the device simulation are approximate doping profiles, simplified physical models, neglect of 3-D effects, etc. In fact, physics-based process and device simulation usually has a lower accuracy as compared to circuit-level device modeling, and it is surely faster and easier to perform a small adjustment of the final circuit than to calibrate the physical models to such high accuracy.

Finally we present an example of phototransistor, where one of the inputs is the photogeneration of electron-hole pairs. The device doping and principle of operation is illustrated in Fig. 12. The light-collection region is about 1 μm wide, and is almost fully depleted at a collector-to-emitter voltage of 10 V. The base terminal is left open. When the device is uniformly illuminated, electron-hole pairs are generated throughout the material. The current I_1 due to holes generated in the base-collector depletion region is injected into the base, and multiplied by the transistor

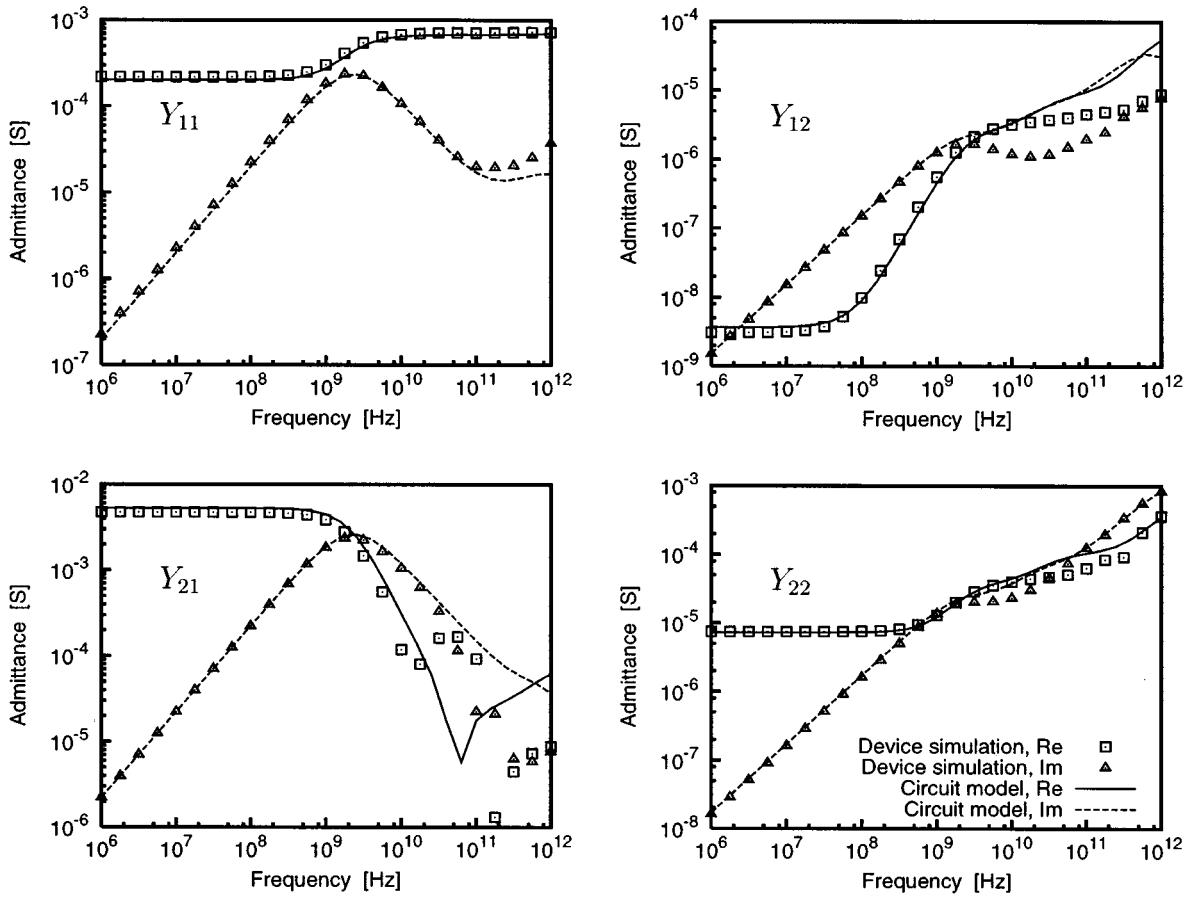

Fig. 11. Frequency dependence of the real and imaginary parts (absolute values) of the Y parameters for a 0.25-μm npn bipolar transistor at a current density of 430 μA/μm^2 ($f_T = 16$ GHz, $f_{\max} = 30$ GHz). Note that the transconductance $G_{21} = \mathrm{Re}[Y_{21}]$ becomes negative around 70 GHz.

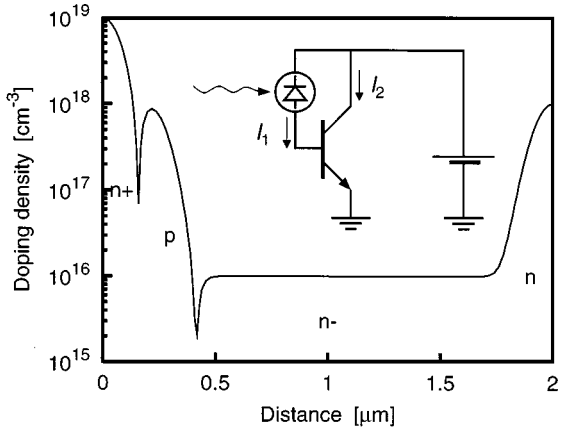

Fig. 12. Doping profile of npn phototransistor. The uniformly doped collection region is about 1 μm wide. The inset shows the schematics of device operation.

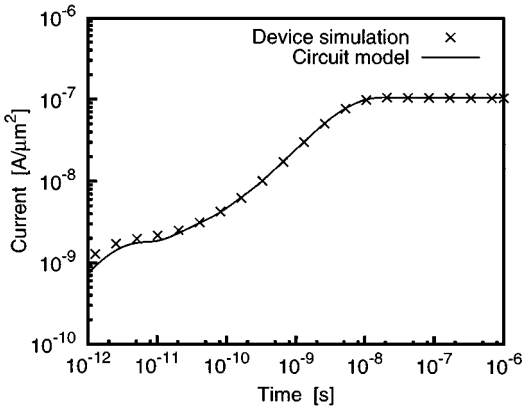

Fig. 13. Time transient of output current for the phototransistor of Fig. 12, for a step increase of light intensity. The initial small increase of current (in the picosecond range) is due to the arrival of primary photocurrent I_1 to the collector, while the second step (reaching saturation at about 10^{-8} s) is due to the current $I_2 = \beta I_1$ by transistor action.

current gain β (Fig. 12, inset). The amplified current $I_2 = \beta I_1$ reaches the collector after a delay due to the charging of the base-emitter junction.

Since the optical response was of interest in this case, the circuit extraction was performed with a single optical stimulus, computing the electrical response to a 10% increase in the light intensity. The extraction method is otherwise identical to that employed for the pn junction example. The time response of the output current to a step increase in optical intensity is shown in Fig. 13. The circuit model tracks the device simulation quite well, including the time delay of 10 ns due to charging of the base-emitter capacitance. Note that the small amplitude of the stimulus allowed in this case a linear analysis of the transient. For a larger optical input, a large-signal model would have been necessary.

VI. Conclusions

In this paper, we have presented a systematic methodology for the generation of physically based equivalent circuit models for semiconductor devices. The 1-D implementation of the technique has been discussed in detail, describing an algorithm for deriving small-signal circuit elements from dc device simulations. Examples for pn junctions and bipolar devices have been presented, showing accurate match between direct ac simulation and the frequency response of the automatically extracted equivalent circuits. Since carrier photogeneration is naturally included in the physically based models, equivalent circuits can be also derived for optoelectronic devices.

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References

[1] K. Doganis and D. L. Scharfetter, "General optimization and extraction of IC device model parameters," *IEEE Trans. Electron Devices*, vol. ED-30, pp. 1219–1228, Sept. 1983.

[2] T. Shima, "Table lookup MOSFET capacitance model for short-channel devices," *IEEE Trans. Computer-Aided Design*, vol. CAD-5, pp. 624–632, Oct. 1986.

[3] W. M. Coughran, W. Fichtner, and E. Grosse, "Extracting transistor charges from device simulation by gradient fitting," *IEEE Trans. Computer-Aided Design*, vol. 8, pp. 380–394, Apr. 1989.

[4] P. B. L. Meijer, "Fast and smooth highly nonlinear multidimensional table models for device modeling," *IEEE Trans. Circuits Syst.*, vol. 37, pp. 335–346, Mar. 1990.

[5] F. Filicori, G. Vannini, and V. A. Monaco, "A nonlinear integral model of electron devices for HB circuit analysis," *IEEE Trans. Microwave Theory Tech.*, vol. 40, pp. 1456–1465, July 1992.

[6] A. Rofougaran and A. A. Abidi, "A table lookup FET model for accurate analog circuit simulation," *IEEE Trans. Computer-Aided Design*, vol. 12, pp. 324–335, Feb. 1993.

[7] S. Mohan, J. P. Sun, P. Mazumder, and G. I. Haddad, "Device and circuit simulation of quantum electronic devices," *IEEE Trans. Computer-Aided Design*, vol. 14, pp. 653–662, June 1995.

[8] F. Filicori, G. Ghione, and C. Naldi, "Physics-based electron device modeling and computer-aided MMIC design," *IEEE Trans. Microwave Theory Tech.*, vol. 40, p. 1333, July 1992.

[9] C. Fiegna, "Physics-based analysis of RF performance of small geometry MOSFETs: Methodology and application to the evaluation of the effects of scaling," *IEDM Tech. Dig.*, pp. 543–546, 1999.

[10] S. Luryi, "Development of RF equivalent circuit models from physics-based device models," in *Future Trends in Microelectronics*, S. Luryi, J. Xu, and A. Zaslavsky, Eds. New York: Wiley, 1999, pp. 463–466.

[11] A. Pacelli, M. Mastrapasqua, M. A. Alam, and S. Luryi, "Automatic generation of equivalent circuits from device simulation," in *Proc. 3rd Int. Conf. Modeling and Simulation of Microsystems*, San Diego, CA, Mar. 2000, pp. 337–340.

[12] C. T. Sah, "The equivalent circuit model in solid-state electronics—III. Conduction and displacement currents," *Solid-State Electron.*, vol. 13, pp. 1547–1575, 1970.

[13] J. G. Linvill, "Lumped models of transistors and diodes," *Proc. IRE*, vol. 46, pp. 1141–1152, June 1958.

[14] C. T. Sah, "New integral representations of circuit models and elements for the circuit technique for semiconductor device analysis," *Solid-State Electron.*, vol. 30, pp. 1277–1281, 1987.

[15] F. A. Lindholm and C. T. Sah, "Circuit technique for semiconductor-device analysis with junction diode open circuit voltage decay example," *Solid-State Electron.*, vol. 31, pp. 197–204, 1987.

[16] H. E. Maes and C.-T. Sah, "Application of the equivalent circuit model for semiconductors to the study of Au-doped p-n junctions under forward bias," *IEEE Trans. Electron Devices*, vol. ED-23, pp. 1131–1143, Oct. 1976.

[17] R. S. Varga, *Matrix Iterative Analysis*. Englewood Cliffs, NJ: Prentice-Hall, 1962.

[18] S. E. Laux, "Techniques for small-signal analysis of semiconductor devices," *IEEE Trans. Electron Devices*, vol. ED-32, pp. 2028–2037, Oct. 1985.

[19] C. L. Ma, P. O. Lauritzen, P.-Y. Lin, I. Budihardjo, and J. Sigg, "A systematic approach to modeling of power semiconductor devices based on charge control principles," in *Conf. Rec. IEEE Power Engineering Specialists* , 1994, pp. 31–37.

[20] Y. Subramanian, P. O. Lauritzen, and K. R. Green, "A compact model for an IC lateral diffused MOSFET using the lumped-charge methodology," presented at the Int. Conf. Modeling and Simulation of Microsystems, San Juan, Puerto Rico, Apr. 1999.

[21] R. B. Schilling, "A regional approach for computer-aided transistor design," *IEEE Trans. Education*, vol. 12, pp. 152–161, Sept. 1969.

[22] ——, "A bipolar transistor model for device and circuit design," *RCA Rev.*, vol. 32, pp. 339–371, Sept. 1971.

[23] G. Aaronson and R. B. Schilling, "A comparison of two transistor models," *IEEE Trans. Electron Devices*, vol. ED-19, pp. 1–3, Jan. 1972.

[24] ——, "A mathematical foundation for linear lumped modeling techniques," *Solid-State Electronics*, vol. 18, pp. 301–308, 1975.

[25] M. R. Pinto, "Simulation of ULSI device effects," *VLSI Sci. Technol.*, vol. 91-11, pp. 43–51, 1991.

[26] S. E. Laux and K. Hess, "Revisiting the analytic theory of p–n junction impedance: Improvements guided by computer simulation leading to a new equivalent circuit," *IEEE Trans. Electron Devices*, vol. 46, pp. 396–412, Feb. 1999.

[27] J. J. H. van den Biesen, "Modeling the inductive behavior of short-base p-n junction diodes at high forward bias," *Solid-State Electron.*, vol. 33, pp. 1471–1476, 1990.

[28] Y.-F. Chyan *et al.*, "A 50-GHz 0.25-μm implanted-base high-energy implanted-collector complementary modular BiCMOS (HEICBiC) technology for low-power wireless-communication VLSIs," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting*, 1998, pp. 128–131.

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