Future Trends in Microelectronics [ISBN 0-471-32183-4] Wiley-Interscience
Edited by S. Luryi, J. M. Xu, and A. Zaslavsky, (New York 1999) pp. 463-466

Development of RF equivalent circuit models from physics-based device models

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Conventional RF modeling of device behavior is done by fitting parameters of a pre-conceived model of a given device (for example, the Ebers-Moll model of a bipolar transistor) to empirical RF data (e.g, measured scattering parameters). This approach fails in at least three situations:

- when one deals with a new type of device for which the device physicists have not done their homework;
- when miniaturization of standard devices brings about new physical phenomena not accounted for by the pre-conceived model; this situation is all too familiar and ranges from short-channel effects in a single MOS transistor to mutual interference between several closely spaced devices to effects of packaging and environment;
- when the device operation is stretched into a new regime, where the old pre-conceived model does not work; this situation includes high-power and/or high-frequency operation, operation in an unusual physical environment, such as magnetic field, incident radiation, etc.

Modern device modeling codes enable the designer to simulate the behavior of nearly arbitrary 3-dimensional semiconductor device structures with multiple electrodes. However, the output of such programs is not a lumped element model that can be used in the design of RF circuits. Rather, such programs produce a (hopefully) good simulation of an experimental situation, as described by the device static and RF characteristics. As far as RF modeling is concerned, the conventional use of device simulators boils down to imitating the RF scattering experiment from which one can obtain parameters of a pre-conceived lumped-element model. Clearly, this procedure suffers from the same limitations as fitting to experiment. I would like to discuss a different approach to this problem, based on physical device modeling without any pre-conceived circuit topology.

A good device modeling program solves semiconductor transport equations together with Poisson's equation and produces files that describe all the internal fields in the device, viz. the potential $V(\mathbf{x})$, the concentrations $n(\mathbf{x})$ and $p(\mathbf{x})$ of electrons and holes, the effective carrier temperatures $T_e(\mathbf{x})$ and $T_h(\mathbf{x})$, as well as temporal variations of these fields. The solutions are usually discretized on a large grid, which in a modern simulator may involve million of nodes. In a sense, such a grid may be viewed as an extremely complicated equivalent network.

We should be able to extract workable equivalent circuit elements by a systematic reduction of the solution files -- appropriately lumping together different nodes that are seen to be at the same potential, replacing streams of current by resistors, etc. Of course, this is precisely what a device physicist is doing implicitly while constructing an equivalent circuit based on a physical picture of the device. Our goal should be to *automate* this process! Ultimately, we need a robust procedure that would act as a postprocessor to device simulators -- producing an equivalent circuit of any desired complexity to any multi-terminal semiconductor structure under any operating conditions, that the device simulator itself can model.

The range of validity of silicon device modeling is rapidly expanding to include new effects, such as those associated with heterostructure discontinuities and non-Boltzmann transport of hot-electrons. Also, device simulations have been successfully applied to electronic transport in compound semiconductor devices, and even to heterostructure lasers. Numerical accuracy of the simulation is not universally reliable in these unconventional regions of application, but qualitatively one often gets a good insight into the physics of device behavior.

In the approach proposed here, the relation between the physical picture provided by the simulator and that which exists in the real silicon structure is not to be challenged. Instead, we should take the simulator model as *infallible* and investigate means for reducing that model to an equivalent circuit.

While it is reasonably clear how to lump the simulator's grid nodes together into elements of capacitive, resistive, or inductive nature, the nature of current *generators* is less clear. Here, I am talking about *control generators*, which force a definite current through a branch of the lumped element circuit in response to a current (or voltage) condition at a different element of the circuit. For example, the Ebers-Moll model of a bipolar transistor contains the generator $G[I_e(I_b)]$ of emitter current controlled by the base current [1]. Similarly, an equivalent circuit of field-effect transistors usually contains a generator $G[I_{ch}(V_G)]$ of channel current controlled by the gate voltage [2]. How should such generators emerge during our simplification of the simulator's solution file?

One approach is to investigate nonlocal correlations between nodes. Perhaps, one can also employ control theory methods and seek local negative differential impedance as a manifestation of one local region in the semiconductor device being controlled by another region. This latter approach is illustrated in Fig. 1.

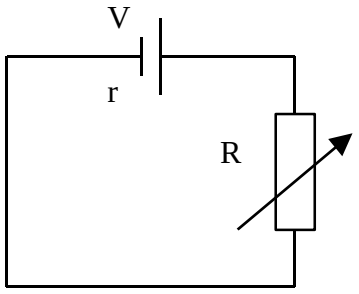

Fig. 1. Let the is externally controlled resistor R suffer a variation dR. Then the variation dV_R of the voltage drop on R will always be of opposite sign to the variation of current dI in the circuit. This negative "impedance" may serve as an indicator of an external control.

For example, we may consider the simulation of a MOS transistor and compute the variational "impedance" $\Re \equiv dV_{ch}/dI$ in response to (a) variation dV_G of the gate voltage and (b) variation dV_D of the drain voltage. As evident from the simple circuit in Fig. 1, in case (a) we find $\Re < 0$, which indicates that channel is controlled by the gate. In contrast, for case (b) we shall find $\Re > 0$, except for second-order effects associated with the small amount of control of the channel impedance by the drain voltage. It appears feasible to develop a robust procedure for identifying the generators in this way.

Another fundamental question to which we would like to provide an answer is when does the topology of an equivalent circuit change? Here, we do not mean incremental changes, such as a negligible capacitance at low frequencies becoming important at higher frequencies, but true topological discontinuous changes in the equivalent circuit, in response to a continuous variation of external parameters, such as the dc voltage, etc. We surmise that such changes will be associated with changes in the topology of equipotential surfaces and current networks in the full solution and recognizing these should involve some form of pattern recognition.

It seems that we should be able to obtain practical answers to such fundamental questions. Ultimately, we would like to develop a robust procedure that would act as a postprocessor to a comprehensive device simulator, producing an equivalent circuit of any desired complexity to any multi-terminal semiconductor structure under any operating conditions, that the device simulator itself can model.

I would like to emphasize again that this approach is radically different from the conventional ways of using a simulator to develop an equivalent circuit. What is done today is simply using the simulator as a convenient "experiment in the bottle" which may be more convenient than to use experimentally derived scattering parameters in that there is no question as to what is and what is not included in the consideration. That may simplify the guess of the equivalent circuit topology, but still the choice of topology requires an expert guess. Making the guess itself is in a sense external to the conventional RF model development process. Of course, if the guess is wrong, no fitting of lumped-element parameters will help. This being used as a feedback to the expert is the current preferred mode of circuit model development. In contrast, we are mainly concerned with automating the choice of topology. If the choice is made right, parameter validation should be quite routine.

Acknowledgement. This work is supported by a grant from the NSF/Industry Center CDADIC [http://www.eecs.wsu.edu/~cdadic/]

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