Active Packaging: a New Fabrication Principle for High Performance Devices and Systems

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1. Introduction

In this work I shall discuss a new device fabrication principle which I would like to refer to as *active packaging* (AP). The meaning of this term is that certain essential fabrication steps (lithography, etching, metallization, etc.) are performed *after* the partially processed device or circuit is packaged onto a host platform.

One of the most important goals of the AP concept is the combination of dissimilar materials (notably, III-V compound semiconductors) with silicon integrated circuitry (IC) on a single Si substrate [1]. This goal, now widely recognized as an important research direction in microelectronics, is shared by other emerging technologies, such as those based on *heteroepitaxial* and *thin-film transfer* techniques [2]. At the same time, AP *widens* significantly the class of device structures that can be manufactured. Our ultimate goal is not only to "teach the old dog new tricks" but also to greatly expand the assortment of tricks available.

It is worth stressing that the word "packaging" is used somewhat unconventionally in the AP context. Active packaging is a device fabrication technique, intended to implement devices on a foreign (not necessarily even semiconductor) platform that perform better than conventionally fabricated devices on their natural semiconductor substrates. In many instances, AP enables the implementation of structures that cannot be realistically obtained in another way, such as those requiring lithography on *opposite* sides of a thin semiconductor film.

The principle of active packaging will be illustrated in the instance of a heterostructure bipolar transistor (HBT) structure, schematically shown in Fig. 1. Such a structure would reduce the parasitic capacitance between the base and the collector electrodes, enabling ultrafast operation with oscillation frequencies in the range of 300-400 GHz and even higher. This in turn would open up the possibility of implementing on-chip millimeter-wave phased-array antenna systems [3].

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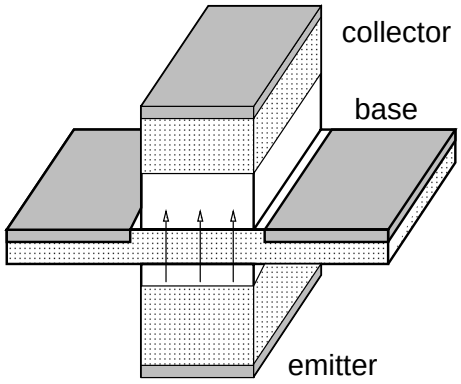

Fig. 1. Idealized cross-section of a heterostructure bipolar transistor to be fabricated by active packaging. Dotted pattern indicates the conducting (undepleted) layers, shaded pattern the contact metal. The emitter and the collector stripes are defined by independent lithographic steps and aligned to each other. If the upward direction is defined as that outward from the surface on which the lithography is performed, then both the emitter and the collector can be considered "up".

2. Active Packaging HBT Process

The process is based on flip-chip packaging, removal of the substrate, and backside lithography. Fabrication begins with the following epitaxial structure:

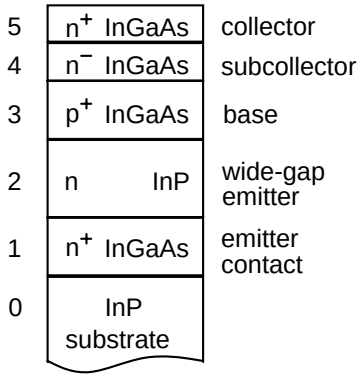

Fig. 2. Epitaxial structure of InGaAs/InP HBT to be fabricated by active packaging. The emitter contact layer 1 is also an etch stop for InP. For etch-stop reliability it may be convenient to include a pair of sacrificial InP-on-InGaAs layers between layers 0 and 1, so that the etching is performed in steps and results in uncovering an ideal flat surface of the emitter contact.

Top side processing includes etching of the collector stripe down to the base layer, evaporation of self-aligned contacts to the base, deposition of a passivating dielectric, etching of via holes and metallization. At this point all the base and collector contacts are connected in a circuit with lines running over the passivating dielectric. The circuit is then covered by another ("interlevel") dielectric layer and a relatively small number of selected points of the circuit are connected to "top" metal pads through a second set of via holes. The top ("communication") pads may be relatively wide (e.g., $\gtrsim 100\ \mu m$). The interlevel dielectric (e.g., polyimyde) may be planarized. No attempt is made at this stage to contact the emitter.

Flip-chip mount; "***consulator***" ***film***. The circuit is then mounted on a "carrier" wafer which has a mirror pattern of metallic communication pads. The carrier may be any substrate, including glass, ceramics, etc., but first and foremost a silicon wafer that has already undergone the integrated circuit processing. Connection between communication pads is established with the help of an anisotropically conducting film with electrical properties, illustrated in Fig. 3. The film must provide a short between overlapping contacts and an open circuit otherwise. Such vertically conducting and laterally insulating films, which may be called "consulators", can be prepared in a variety of ways. The primary purpose of the consulator, besides providing vertical electrical connections, is to provide a stable mechanical support for the packaged chip – support that will become crucial when the InP substrate is removed.

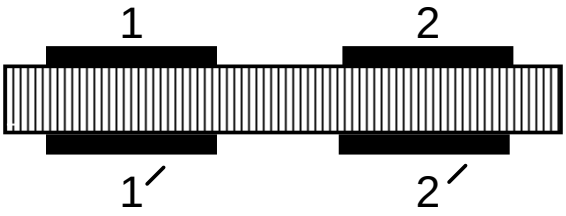

Fig. 3. Required "consulator" film. For overlapping electrodes the film provides a short, $R(11') \approx R(22') \lesssim 10\,\Omega$, while nonoverlapping electrodes form an open circuit, $R(12) \approx R(12') \gtrsim 10^8\,\Omega$.

In principle, a perfectly adequate consulator can be provided by the solder-bump technology. One needs an adhesive dielectric that can flow to fill the narrow spacing between the chip and the carrier wafer and then stiffen to provide the necessary mechanical support. Another possible approach is to use the existing packaging technology of anisotropically conductive adhesive films, used in liquid crystal display assemblies. These materials are not intrinsically anisotropic, they conduct in a preferred direction only after having been processed, Fig. 4.

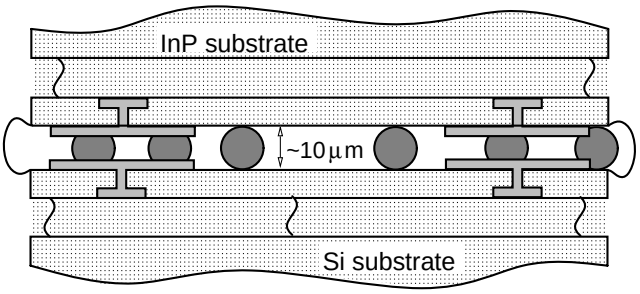

Fig. 4. Anisotropically conductive adhesives (after Ref. [4]). Small conducting spheres are dispersed in an epoxy matrix at a concentration below the percolation threshold for electric conductivity. The assembly is compressed until hard spheres touch both surfaces (extra epoxy oozes out). Electrical connection is established only vertically, since neighboring spheres rarely touch.

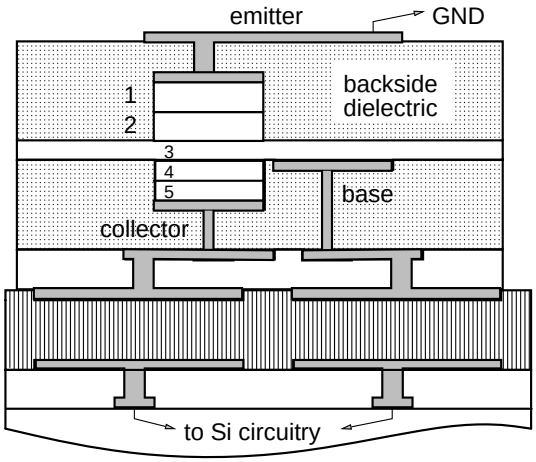

Fig. 5. Cross-section of the final assembly after active packaging. Emitter stripe is aligned to and slightly overlaps the collector stripe. It is assumed for simplicity that all HBT's are used at common emitter, so that the emitter final metal is connected to the ground of the Si circuit. Of course, this may not be true in general, and the emitter final metal pattern may be more complicated. Connection to the rest of the circuit may go across the periphery of the chip, or via the consulator film.

Substrate removal and back-side processing. It is quite possible to etch the entire InP substrate down, stopping at a 0.1 μm InGaAs layer. This step is based on the well-known extreme selectivity between the etch rates for InP and InGaAs in hydrochloric acid solutions. It is essential that the uncovered surface of layer 1 is uniformly flat, adequate for performing a fine line optical lithography. A large hole etched from the substrate side would not do, because there would be problems with focal depth. To make lithographic alignment to the base contact level, the contact metal should be seen with a sufficient contrast through layers 1-3. If this proves to be inconvenient, then special topography features for the back-side alignment must be provided at the top-side processing stage.

The final assembly is illustrated in Fig. 5. The emitter contact is established by a standard lift-off evaporation of a suitable metal. It is well known that ohmic contacts to n^+ InGaAs are good without alloying. No elevated temperature procedures should be contemplated after the chip has been mounted, because of the limited thermal stability that can be expected of a consulator film and the need to preserve the integrity of fully processed Si integrated circuits on the carrier wafer.

3. Advantages

The reduced base-collector capacitance offers significant advantages for microwave performance of HBT. An enhancement of the maximum oscillation frequency $f_{\max}$ by a factor of 2 to 3 has been predicted [5,6] over optimized collector-down structures. Moreover, with a suppression of the extrinsic collector capacitance C_{Cx} it becomes possible to implement HBT structures with *coherent* effects in the base [7,8], resulting in a power gain above the conventional cutoff frequencies. Figure 6 shows the modeled microwave characteristics of a collector-up HBT, in which the base bandgap is graded so that the total base propagation delay τ is much shorter than the diffusive delay in a flat base of the same width [8]. The magnitude of the base transport factor $\alpha = |\alpha| \exp(-2\pi i f \tau)$ decreases so slowly with increasing frequency f that it becomes feasible to activate transit-time resonances far above $f_T \approx 1/2\pi\tau$. The fundamental peak in U occurs near πf_T [7,8].

The coherent transistor can be designed to have the first high-gain peak at any desired frequency, provided the effect is not destroyed by the parasitics. For frequencies below 100 GHz it is possible to use conventional structures (Fig. 6a), where typically the extrinsic (parasitic) collector capacitance C_{Cx} is about twice the intrinsic (useful) capacitance C_C. In order to push the peak into a sub-millimeter wave range (Fig. 6b) it is essential to reduce C_{Cx} below C_C. The AP process opens a way to substantially reduce the extrinsic capacitance.

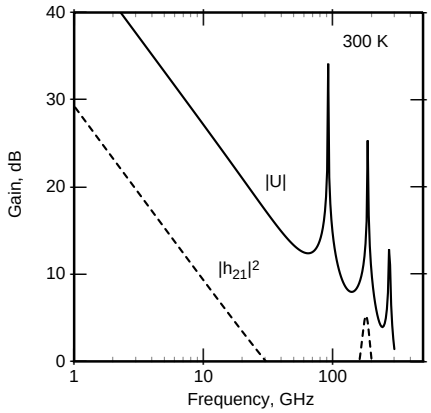

Fig. 6a. Common-emitter current gain $|h_{21}|$ and the unilateral power gain $|U|$ of a model coherent transistor with a special graded-gap base design, optimized for stable oscillation at $94\,\text{GHz}$. Base total width $W = 1\,\mu\text{m}$. Transistor is assumed loaded with the parasitics with state-of-the art equivalent circuit parameters, e.g. $C_{Cx} = 2C_C$. Conventional current-gain cutoff is $f_T \approx 32\,\text{GHz}$, however the transistor also exhibits a range of current gain $|h_{21}| > 1$ at $f \approx 2\pi f_T$ (near the second peak in U). The fundamental peak in U occurs near πf_T (after Refs. [7] and [8]).

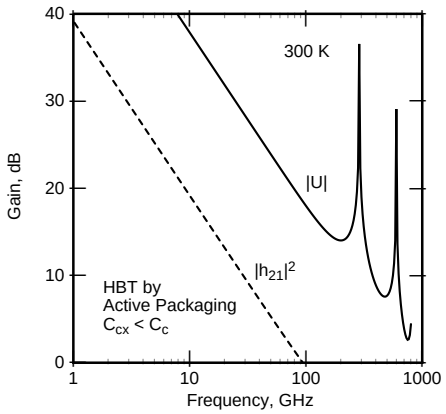

Fig. 6b. Reduction in the parasitic capacitance C_{Cx} by the active packaging process enables a more aggressive design of the coherent transistor, optimized for stable oscillation at near $300\,\text{GHz}$. Base total width $W = 0.3\,\mu\text{m}$. Transistor is assumed loaded with the parasitics with state-of-the art equivalent circuit parameters, except C_{Cx} which is assumed small, $C_{Cx} \leq 0.5C_C$. The minority-carrier diffusivity $D \approx 25\,\text{cm}^2/\text{s}$. The base transit time (by drift) is $\tau_B = 1\,\text{ps}$ and collector transit time $\tau_C = 0.75\,\text{ps}$, resulting in a conventional $f_T \approx 100\,\text{GHz}$.

An interesting further advantage of an AP HBT is the possibility of accommodating a Schottky collector, Fig. 7. An important parasitic resistance in small area devices is due to the metal semiconductor junction. Since the resistance of an ohmic contact scales with its area, at small enough dimensions it must dominate other resistances that scale with the contact perimeter. It therefore makes sense to dispense with the n^+ doped semiconductor layer in the collector (layer 5 in Fig. 2). Such an approach has been successfully used in the fabrication of submicron resonant tunneling diodes [9]. The high thermal conductivity of a metallic layer and its proximity to the n^- base-collector field region, where most of the heat is generated, is another important advantage of a Schottky collector. Needless to say, a Schottky collector is realistic only in a collector-up configuration. Its implementation is entirely compatible with the AP process.

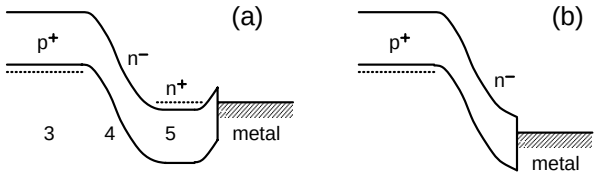

Fig. 7. Illustration of a conventional ohmic semiconductor-metal contact (*a*) and a Schottky collector (*b*). Numbers in (*a*) refer to the layer labeling scheme in Fig. 2. In a Schottky-collector device, layer 5 would be eliminated altogether and a suitable metal deposited directly on the lightly-doped layer 4, completely depleted of mobile carriers.

4. Applications

Based on AP HBT technology it is entirely feasible to implement local oscillators and amplifiers that operate at millimeter and even submillimeter wavelengths. One obvious application of such devices would be for satellite communication systems in the atmospheric transmission window of 345 GHz.

Another extremely attractive application [3] is the possibility of fabricating millimeter-wave *phased arrays on a silicon chip*. A $\lambda/2$ spaced linear array of 20 elements radiating at 300 GHz would be about a centimeter long. The advantage of having transistor oscillators is that the millimeter-wave beam can be electrically steered off broadside by controlling the relative amplitudes of different oscillators, while their relative phases are locked together by the evanescent wave interaction. The point is that most available phase shifters used in centimeter wave phased array systems are bulky elements that cannot be used in on-chip designs. Instead, we should use electronic beam steering by controlling the *amplitude* of constant-phase

array elements [10]. As far as I am aware, this idea has not been employed in practical phased-array antenna systems, perhaps because at centimeter wavelengths it is more efficient to control the relative phases of array elements. In the millimeter and submillimeter wavelength range amplitude steering appears to be the only realistic way to implement purely electronic beam steering. Three-terminal devices are ideally suited for this purpose. On-chip focal plane antenna arrays should have important applications as steerable radar systems in avionics, automated manufacturing, and especially in automobile collision avoidance and early warning systems.

5. Conclusion

Generality of the active packaging principle transcends microwave transistor applications. The new degree of freedom in manufacturing – lithography on opposite sides of a thin film – permits the implementation of a variety of new devices and functions. Of the many possible examples, let me mention the possibility [11] of fabricating a collector-up charge injection transistor with the channel-defining trench etched in side 2 and aligned to the collector stripe on side 1. To indicate the scope of contemplated applications, let us note that the technique makes feasible an active directional coupler in which two edge-emitting laser resonators overlap in a portion of their length. It also simplifies many schemes for integrating electronic and photonic devices into a single functional unit to be placed within the integrated circuitry on a silicon chip.

Vertical cavity surface emitting lasers (VCSEL) should have an important role in this program, because such elements enable interchip communication directly from the chip interior. Active packaging technology offers several advantages in the integration of VCSELs with silicon VLSI. For example, it allows to use *non-epitaxial* Bragg mirrors (such as stacks of ZnS and SiO_2 layers) not only for the top but also for the bottom mirror of a VCSEL cavity. Also it permits the implementation of *tandem systems* in which one VCSEL (master) works under electrical injection of carriers while the other (slave) is optically pumped by the former.

I believe that most significant applications of compound semiconductor electronics will be associated with its use in silicon electronics. In terms of the old debate on Si vs GaAs, my view is that silicon is the ultimate customer for GaAs. The logic of industrial evolution will motivate new paths for a qualitative improvement of system components, other than the traditional path of a steady reduction in fine-line feature size. The principle of active packaging, illustrated in the present work using the instance of implementing ultra-high performance InP HBT on a silicon chip, will become one of the central design principles of future microelectronics.

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