How to Make an Ideal HBT and Sell It Too

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***Abstract*—New technology of *active packaging* (AP) is proposed. It permits the implementation of device structures that require lithography on *opposite* sides of a thin semiconductor crystal layer. A major goal of the AP technology is to integrate III-V devices with silicon integrated circuitry on a single substrate; the purpose, however, is not only to "teach the old dog new tricks" but also to greatly expand the assortment of tricks available. The concept is illustrated by describing a process for the fabrication of a collector-up InP heterojunction bipolar transistor, capable of oscillation in the frequency range of 300–400 GHz. An attractive application for this technology is the implementation of millimeter and submillimeter phased antenna arrays, in which beam steering is accomplished by amplitude modulation of array elements at a fixed phase difference. Focal plane antenna arrays on a silicon chip should have important applications in automobile collision avoidance and early warning systems, as well as satellite communication systems.**

I. Introduction

It has been long recognized [1]–[3] that a significant improvement in the high-frequency performance of heterojunction bipolar transistors (HBT) can be expected from a technology that would offer a practical way of implementing a collector-up (C-up) structure. The advantage of an inverted structure results mainly from a reduction in the parasitic base-collector capacitance, associated with the extrinsic base region, Fig. 1. In a conventional emitter-up HBT, Fig. 1(a), this parasitic capacitance is hard to avoid (although attempts have been made [4] to bury implanted isolation layers underneath the base contact). The key to a successful implementation of C-up HBT's is to reduce the parasitic injection of minority carriers in the extrinsic base region, Fig. 1(b). One way of doing this, proposed by Kroemer [1], is to form a PN junction in the wide-gap emitter layer, that would have a higher built-in potential barrier than the injecting NP junction under the collector. Another approach was first demonstrated by Adachi and Ishibashi [5], who adapted the O^+ implantation technique [4] to form a buried isolation layer. Subsequently, implanted O^+ layers blocking the parasitic injection in the extrinsic base-emitter junction have been used in the fabrication of C-up microwave HBT's both in GaAs/AlGaAs [6] and InP-based technologies [7], [8].

In this work a different approach to the implementation of HBT's with reduced parasitics is discussed. This approach is based on a new device fabrication principle which the author would like to refer to as *active packaging*. The meaning of this term is that certain essential fabrication steps (lithography, etching, metallization, etc.) are performed *after* the partially processed device or circuit is packaged onto a host platform. In many instances, active packaging (AP) will permit the implementation of structures that cannot be realistically implemented in another way, such as those requiring lithography on *opposite* sides of a thin semiconductor film.

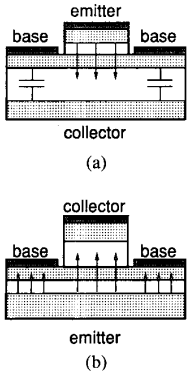

Fig. 1. Schematic cross section of a heterostructure bipolar transistor. Dotted pattern indicates the conducting (undepleted) layers. In the conventional emitter-up structure (*left*) the extrinsic part of the base-collector junction under the base contact has a large parasitic capacitance. Implementation of a collector-up structure (*right*) requires suppressing the minority-carrier injection outside the collector area (indicated by the short arrows).

An essential ingredient of active packaging is an anisotropically conducting film with electrical properties, schematically illustrated in Fig. 2. The film must provide a short between overlapping contacts and an open circuit otherwise. The minimum required overlap area and distance between non-overlapping electrodes should not be too large, preferably less than 100 μm. Such vertically conducting and laterally insulating films may be called "consulators" (or "insuductors"). As will be discussed in Section III, such films can be prepared in a variety of ways, some of which are readily available, others can be expected to result from further research. A consulator film with suitable thermomechanical properties enables a flip-chip bonding of a partially processed (on side 1) compound semiconductor chip to a carrier wafer. Subsequently, the exposed substrate surface (side 2) of the chip is etched back to an etch-stop layer within a few microns from side 1. The uncovered flat surface is then suitable for a side 2 lithography defining fine-line features aligned to those on side 1. The bond and etchback process has a conceptual similarity with recent techniques developed for Si on insulator (SOI) applications [9]; however, as far as the author knows, the alignment of features defined by opposite-side lithographies has not been contemplated in the SOI development—in part because no currently available epitaxial layer on Si has the required extreme etch selectivity against silicon.

Manuscript received March 3, 1994. The review of this paper was arranged by Associate Editor J. Xu.

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IEEE Log Number 9405956.

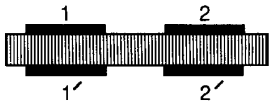

Fig. 2. Anisotropically conducting "consulator" film required for active packaging. The film shorts overlapping electrodes, $R(11') \approx R(22') \leq 10\,\Omega$, while nonoverlapping electrodes form an open circuit, $R(12) \approx R(12') \geq 10^8\,\Omega$.

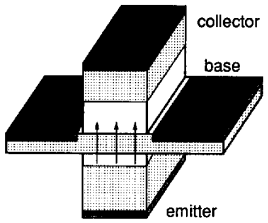

Fig. 3. Idealized cross section of a heterostructure bipolar transistor to be fabricated by active packaging. Dotted pattern indicates the conducting (undepleted) layers, shaded pattern the contact metal. The emitter and the collector stripes are aligned to each other.

In the next Section, an AP process resulting in the formation of a HBT structure, schematically shown in Fig. 3 is described. Since both the emitter and the collector stripes are defined by independent lithographic steps and aligned to each other, it is rather immaterial which one is up; moreover, if the definition of upward direction is outward from the surface on which the lithography is performed, then both the emitter and the collector are "up."

Generality of the active packaging concept transcends bipolar transistor applications. One of its most important goals is the combination of dissimilar materials (notably, III-V compound semiconductors) with silicon integrated circuitry (IC) on a single Si substrate [10]. This goal, now widely recognized as an important research direction in microelectronics, is shared by other emerging technologies, such as those based on *heteroepitaxial* and *thin-film transfer* techniques (see [11] for a recent review). At this time, the potentially very promising field of III-V heteroepitaxy on Si is still focusing on the materials quality issues. Thin-film transfer technologies have attracted considerable attention after Yablonovitch *et al.* [12] demonstrated a viable epitaxial lift-off (ELO) technique for peeling off and transplanting large-area high-quality thin films of GaAs. The film separation is based on a high selectivity (10^8 in a hydrofluoric acid solution) of etching AlAs compared to GaAs. Current issues of concern in ELO technologies [13] are related to the bonding of thin films to a new substrate, viz. their adhesion, alignment, stress, etc.

The AP technology, as I envisage it, shares its major goal of integrating III-V devices in silicon IC's with both the heteroepitaxy and the ELO. At the same time, it *widens* significantly the class of device structures that can be manufactured. The ultimate goal of AP is not only to "teach the old dog new tricks" but also to greatly expand the assortment of tricks available. One possibility in this regard is the implementation of a millimeter (or submillimeter) wave phased-array antenna system on a silicon chip, discussed in Section IV.

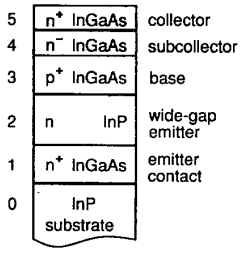

Fig. 4. Epitaxial structure of InGaAs/InP HBT to be fabricated by active packaging. The emitter contact layer 1 is also an etch stop for InP. For etch-stop reliability it may be convenient to include a pair of sacrificial InP-on-InGaAs layers between layers 0 and 1.

II. Collector-Up HBT Process

The process is based on flip-chip packaging, removal of InP substrate, and backside lithography. Fabrication begins with an epitaxial structure of the following composition:

The structure shown in Fig. 4 is, of course, very schematic; it is assumed that most of the features improving the performance of a "conventional" down-collector InP/InGaAs microwave HBT [14] can be incorporated. Thus the base collector junction may have a composite structure for optimizing the microwave properties combined with higher breakdown voltage [15]. An additional attractive feature that becomes possible *only* in a C-up process is a *Schottky collector*, discussed in Section II-E.

Composition of the emitter contact layer 1 is essential: it is intended to serve also as an etch stop for subsequent removal of InP substrate. It may be advantageous to include for this purpose a pair of sacrificial InP/InGaAs layers between layers 0 and 1, so that the etching is performed in steps and results in uncovering an ideal flat surface of the emitter contact.

A. Top Side Processing

No attempt is made at this stage to contact the emitter. Top side processing includes metallization and etching of the collector stripe down to the base layer, evaporation and alloying of self-aligned contacts to the base, deposition of a passivating dielectric (e.g., Si_3N_4), etching of via holes in the dielectric, and final metallization. The final metal connects different devices in a circuit that has a relatively small number of communication points with the outside world. The circuit is then covered by another ("interlevel") dielectric layer and the communication points are connected to "top" metal pads through a second set of via holes. The top pads may be relatively wide (e.g., $\gtrsim 100\,\mu$m). The interlevel dielectric (e.g., polyimyde) may be planarized. It may prove convenient to use ion implantation in the base area outside the collector stripe so that the PN junction in that area is formed in the wide-gap layer 2.

B. Flip-chip Mount

The circuit is mounted on a "carrier" wafer which has a mirror pattern of top-metal electrodes. The word "mirror" here implies also that heights of the aligned pads should be complementary (elevated pads on the InP chip correspond to

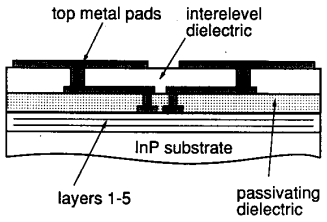

Fig. 5. Cross section of the structure after top-side processing. Base and collector contacts are connected in a circuit with lines running over the passivating dielectric. Selected circuit points are connected with top metal pads through via holes in the interlevel dielectric. Emitter layers are not yet contacted.

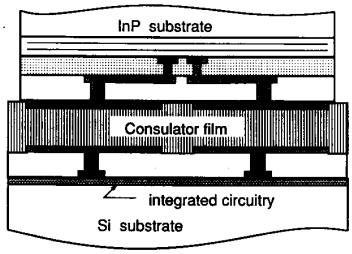

Fig. 6. Cross section of the assembly upon flip-chip mount. Top pads of the InP chip are aligned to a mirror set of pads on the carrier platform. The "mirror" arrangement also implies that the pads have been designed with complementary heights.

depressed pads on the carrier and vice versa). The carrier may be any substrate, including glass, ceramics, etc., but first and foremost a silicon wafer that has already undergone the integrated circuit processing. Connection between overlapping metallic pads is established with the help of a consulator film. Its primary purpose, besides providing vertical electrical connections, is to provide a stable mechanical support for the packaged chip—support that will become crucial when the InP substrate is removed. Possible implementations of the consulator are discussed below in Section III.

C. Substrate Removal

This step is based on the well known extreme selectivity between the etch rates for InP and InGaAs in hydrochloric acid solutions [16]. It is quite possible to etch the entire InP substrate down, stopping at a 0.1 μm InGaAs layer. Prior to etching, the mounted InP chip may be thinned down to less than 100 μm by a mechanical polishing, although this step may not be necessary. While the emitter contact layer 1 itself can serve as the etch stop, it may be preferable to use an additional pair of sacrificial InGaAs/InP layers between the substrate and the emitter contact. It is essential that in the end the uncovered surface of layer 1 is uniformly flat, adequate for performing a fine line optical lithography. A large hole etched from the substrate side would not do, because there would be problems with focal depth. Ideally, the consulator film should be resistant to the HCl based etch of InP. Otherwise, the film would have to be protected on the perimeter.

D. Back-side Processing

It is expected that it should be possible to make lithographic alignment to the base contact level. The contact metal should

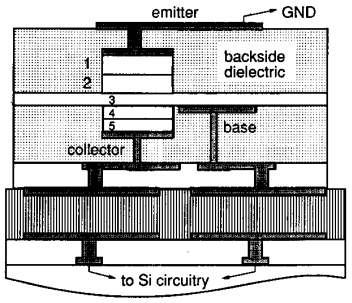

Fig. 7. Cross section of the final assembly after active packaging. Emitter stripe is aligned to and slightly overlaps the collector stripe. It is assumed for simplicity that all HBT's are used at common emitter, so that the emitter final metal is connected to GND of the circuit.

be seen with a sufficient contrast through layers 1–3, whose combined thickness may be about 2000 Å. If this proves to be inadequate or inconvenient, then one must provide for special topography features for the back-side alignment, e.g., a deep alloy penetration of the base contact into layer 2 at the top-side processing stage.

As mentioned in Section II-A, it is helpful to have formed the PN junction in the wide-gap layer 2 outside the collector stripe area. In accordance with the original Kroemer's proposal [1], the PN junction will serve as an efficient guard-ring pushing the injection current density away from the perimeter, since it has a higher potential barrier than the injecting NP junction under the collector contact. This will permit us to employ a *slightly wider emitter stripe, that overlaps the collector stripe* to within a lithographic tolerance.

The emitter contact is established by a standard lift-off evaporation of a suitable metal. It is well known that ohmic contacts to n^+ InGaAs are good without alloying. No elevated temperature procedures should be contemplated after the chip has been mounted, because of the limited thermal stability that can be expected of a consulator film and the need to preserve the integrity of fully processed Si IC's on the carrier wafer. Thus, a dielectric passivating the back surface should be deposited at room temperature. Back-side processing ends with opening via holes in the dielectric and evaporating the final metal pattern. In many applications, the emitter final metal is to be earthed, i.e., connected to the GND level of the Si IC, as indicated in Fig. 7. Of course, this may not be true in general, and the emitter final metal pattern may be more complicated. Connection to the rest of the circuit may go across the periphery of the chip, or via the consulator film.

E. Further Advantages of a C-up Configuration

As discussed by a number of authors [1]–[3], the reduced base-collector capacitance offers significant advantages for microwave performance of HBT. An enhancement of the maximum oscillation frequency $f_{\max}$ by a factor of 2–3 has been predicted [2] over optimized collector-down structures. Moreover, with a suppression of the extrinsic collector capacitance C_{Cx} it becomes possible to implement HBT structures with coherent effects in the base and collector transit, resulting

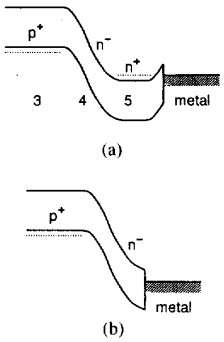

Fig. 8. Illustration of a conventional ohmic semiconductor-metal contact (a) and a Schottky collector (b). Numbers in (a) refer to the layer labeling scheme in Figs. 4 and 7. In a Schottky-collector device, layer 5 would be eliminated altogether and a suitable metal deposited directly on the lightly-doped layer 4, completely depleted of mobile carriers.

in a power gain at frequencies well above the transit-time limited cutoff f_T (see [17], [18] and references cited therein).

An interesting further advantage of an inverted HBT is the possibility of accommodating a Schottky collector. As discussed by Rodwell [19] in the context of resonant tunneling diodes, an important parasitic resistance in small area devices is due to the metal semiconductor junction. Since the resistance of an ohmic contact, Fig. 8(a), scales with its area, at small enough dimensions it must dominate other resistances that scale with the contact perimeter. It therefore makes sense to dispense with the n^+ doped semiconductor layer in the collector (layer 5 in Fig. 4) and use a Schottky collector, Fig. 8(b). Such an approach has been successfully used [20] in the fabrication of submicron resonant tunneling diodes. Needless to say, a Schottky collector is realistic only in the C-up configuration. Its implementation is entirely compatible with the AP process. The high thermal conductivity of a metallic layer and its proximity to the n^- base-collector field region, where most of the heat is generated, is another important advantage of a Schottky collector.

III. Consulator Films

It should be clear from the above discussion in Section II what are the required properties of a consulator film to be used in an AP process. Besides the defining property of anisotropic conduction, illustrated in Fig. 2, we need reasonable mechanical properties to provide a stable and stress-free support for the packaged chip that will be turned into a thin film.

A. Artificial Films

In principle, it should be possible to extend a solder bump technology, as illustrated in Fig. 9. In this approach, the unresolved issue is how to provide a solid adhesive support of the top film over the entire area. After the AP process, the film will be thin indeed, a few μm at most, spanned across hundreds of μm between the bumps. It is therefore crucial to find a suitable substance that could flow to fill the narrow spacing between two planes and then stiffen to provide the necessary mechanical support. Recently, a very interesting contribution in this regard was made by Goossen *et al.* [21] who used an

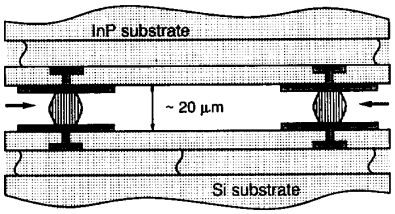

Fig. 9. Converting solder bumps into a "consulator" film. Is it possible to fill (as shown by two arrows) the space between the chip and the carrier wafer by a flowing dielectric adhesive which can then be hardened by a suitable curing treatment?

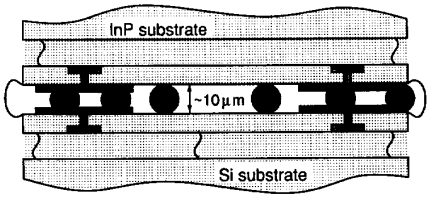

Fig. 10. Illustration of anisotropically conductive adhesive technology [22]. Epoxy filled with 10 μm-diameter metal-coated glass spheres is spread over the carrier wafer surface as a fluid film about 20 μm thick. The assembly is compressed until hard spheres touch both surfaces (extra epoxy oozes out). Electrical connection is established only vertically, since neighboring spheres rarely touch.

aligned mirror arrangement of In contacts, melted into each other at 200°C to form a stable unit. The clearance between samples was filled with a photoresist flowing against the edge of the assembly; the resist was then hardened by drying in the air. According to the authors [21], the resist provided additional mechanical support to the assembly.

If a suitable filling dielectric can be found and technologically proven, then solder-bonded technology should be perfectly adequate for active packaging. Another promising approach is to use the existing packaging technology of *anisotropically conductive adhesive films* [22], used in liquid crystal display assemblies. Anisotropic adhesives are prepared by randomly dispersing small conducting spheres in an adhesive matrix at a concentration below the percolation threshold. These materials are not intrinsically anisotropic, they conduct in a preferred direction only after having been processed under pressure, Fig. 10.

B. "Natural" Films

Since 1989 two independent Russian groups have reported [23], [24] that thin films of atactic polypropylene, deposited on metal substrates and subsequently oxidized and UV irradiated, exhibit an unusually high conductivity in the direction perpendicular to the film, while remaining essentially insulating in the lateral direction. The typical resistance measured between overlapping electrodes is about 1 Ω with no relation to the film thickness (in the range from 5 μm to 50 μm) or electrode area (10^{-6} to 10^{-2} cm^2). These properties have been attributed to the existence of narrow (less than 0.1 μm) channels, whose conductivity ($\geq 10^{11}$ S/cm) at room temperature is claimed to

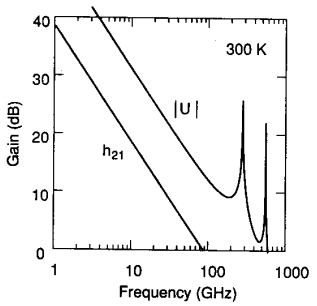

Fig. 11. Common-emitter current gain $|h_{21}|$ and the unilateral gain $|\mathcal{U}|$ of a model HBT with $N = 5$ equal steps in the base bandgap [17]. Base total width is $W = 0.25\,\mu$m. Assumed equivalent circuit parameters: $R_B = R_{Bx} = 50\,\Omega\cdot\mu$m, $R_E = 10\,\Omega\cdot\mu$m, $R_{Ex} = R_{Cx} = 20\,\Omega\cdot\mu$m, $C_C = 0.25\,\text{fF}/\mu$m, and $C_E = 10\,\text{fF}/\mu$m. Minority carrier diffusivity $D = 50\,\text{cm}^2/\text{s}$ and collector transit time $\tau_C = 1$ ps.

exceed that of copper. The nature of these channels is not understood, and speculations [25]–[27] regarding the physical mechanism include suggestions of a one-dimensional superconductivity. Apart from the uncertain theoretical basis, a serious problem for applications had been associated with loose mechanical properties of a tactic polypropylene, which has a gel structure. Professor Leonid N. Grigorov and his group at Moscow Institute of Synthetic Polymer Materials [28] found similar effects in other polymers with better mechanical properties; one most promising material is mechanically similar to rubber.

IV. Applications

Integration of ultra-high performance HBT and silicon circuits will make possible entirely new systems. A collector-up HBT can operate at 300 GHz and even higher frequencies. Fig. 11 shows the modeled microwave characteristics of an InP C-up HBT whose base bandgap narrows down toward the collector in N discontinuous steps [17]. If the potential energy drop at each step is sufficiently large to prevent the reverse flow of minority carriers, the total base propagation delay τ is shorter by a factor of N compared to the diffusive delay in a flat base of the same width. Moreover, for large N the magnitude of the base transport factor $\alpha = |\alpha| \exp(-2\pi i f\tau)$ decreases so slowly with increasing frequency f that it becomes feasible to obtain transit-time resonances at frequencies far exceeding the conventional cut-off $f_T \approx 1/2\pi\tau$. The first resonant peak occurs at $f \approx \pi f_T$ (in the example of Fig. 11, this corresponds to about 280 GHz). The peak frequency is determined mainly by the epitaxial structure, but it can also be tuned in a narrow range.

Thus using AP technology it is entirely feasible to implement local oscillators and amplifiers based on C-up HBT's that operate at millimeter and even submillimeter wavelengths. One obvious application of such devices is for satellite communication systems in the atmospheric transmission window of 345 GHz.

Another extremely attractive application is the possibility of fabricating millimeter-wave *phased arrays on a silicon chip*. A phased array antenna system [29] needs low-noise amplifiers at each element *and* high-power amplifiers at least at each subarray. Local placement of these amplifiers reduces the antenna loss on transmit and enhances the signal-to-noise ratio on receive. The closer the amplifiers are placed to the radiating elements the better is the antenna performance [30]. With the AP technology, the entire system can be placed on a silicon chip. A $\lambda/2$ spaced linear array of 20 elements radiating at 300 GHz would be about a centimeter long.

The advantage of having transistor oscillators is that the millimeter-wave beam can be electrically steered off broadside by controlling the relative amplitudes of different oscillators, while their relative phases are locked together by evanescent wave interaction [31]. The point is that most available phase shifters used in centimeter wave phased array systems are bulky elements that cannot be used in on-chip designs. Instead, we should use electronic beam steering by controlling the *amplitude* of constant-phase array elements. Such an approach has been proposed by Costas [32], who discussed theoretically a beam steering technique using a pair of interleaved arrays, one of which is fed entirely by currents of zero phase the other entirely by currents of quadrature phase. As far as I am aware, it has not been employed in practical phased-array antenna systems, perhaps because at centimeter wavelengths it is more efficient to control the relative phases of array elements. In the millimeter and submillimeter wavelength range amplitude steering appears to be the only realistic wave of purely electronic beam steering.

Although it is recognized that beam steering can also be accomplished by mechanical means as well as optoelectronic means (for example, Froberg *et al.* [33] recently demonstrated a steerable photoconducting antenna array at submillimeter wavelengths), it is expected that purely electronic means for beam steering will prove to be a more convenient and versatile technique. Three-terminal devices are ideally suited for amplitude beam steering. Such transmit and receive antenna arrays should have important applications as steerable radar systems in avionics, automated manufacturing, and especially in automobile collision avoidance and early warning systems, perhaps also in connection with *"intelligent vehicle-highway systems"* [34].

V. Conclusion

I have described a possible technique for implementing ultra-fast InP heterostructure bipolar transistors as elements on a silicon chip. A remarkable feature of this technique, referred to as active packaging, is that it permits the implementation of hybrid devices that are essentially *faster* than similar devices made within the conventional InP technology. The advantage results form the fact that packaging is an *intermediate* step in the device fabrication sequence, and enables subsequent processing with an aligned lithography on the opposite side of a thin film. The new degree of freedom in the device geometry definition permits the implementation of collector-up HBT's with aligned and overlapping emitter and collector stripes.

Of possible applications of active packaging, I have singled out the implementation of microwave phased-array antenna

systems at a wavelength of $\lambda \approx 1\,\mu$m (300 GHz). Transmit and receive millimeter-wave antenna arrays on a silicon chip should have important applications in steerable radar and satellite communication systems.

It is clear that active packaging will make possible the implementation of other new devices and circuits that would not be feasible without this new technology. Of the many possible examples, let me mention the proposal [35] of fabricating a C-up charge injection transistor with the channel-defining trench etched in side 2 and aligned to the collector stripe on side 1. Another possibility is the implementation of vertically coupled dual laser cavities and directional couplers, laterally confined by separate ridges on sides 1 and 2.

I strongly believe that most significant applications of compound semiconductor electronics will be associated with its use in silicon electronics. In terms of the old debate on Si versus GaAs, my view is that silicon is the ultimate customer for GaAs. The logic of industrial evolution will motivate new paths for a qualitative improvement of system components, other than the traditional path of a steady reduction in fine-line feature size. The principle of active packaging, illustrated in the present work using the instance of implementing ultra-high performance InP HBT on a silicon chip, will become one of the central design principles of future microelectronics.

ACKNOWLEDGMENT

The author is grateful to Q. Hu, A. Feygenson, M. P. Lepselter, W. T. Lynch, A. M. Lyons, M. Mastrapasqua, G. L. Miller, F. Ren, I. Shlimak, E. Suhir, J. Wight, and J. M. Xu for helpful discussions and encouragement.

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