COLLECTOR-CONTROLLED STATES IN CHARGE INJECTION TRANSISTORS

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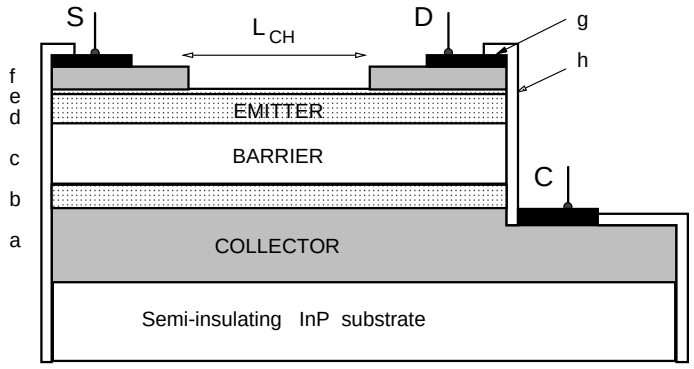
ABSTRACT

We review recent theoretical studies of the symmetry properties of charge injection transistors. These studies, based on continuation modeling and transient device simulation, incorporate self-consistently the electron energy and real-space transfer currents over heterojunction interfaces. Inspection of the full device phase-space reveals a variety of instabilities and a striking novelty of *multiply-connected* current-voltage characteristics. We have found anomalous steady states in which hot-electron injection occurs in the absence of any voltage between the emitter electrodes. In these states, some of which are not only stationary but also *stable* with respect to small perturbations, the electron heating is due to the fringing field from the collector electrode. Some of the anomalous states break the reflection symmetry in the plane normal to the channel at midpoint. The study elucidates the formation of hot-electron domains in real-space transfer.

INTRODUCTION

The charge injection transistor[1] or CHINT is a three-terminal heterojunction device which operates on the principle of real-space transfer[2] (RST) of electrons, heated by a lateral field, over an energy barrier into the adjacent layer. Figure 1 shows a schematic structure of the device,[3] implemented in the $In_{.53}Ga_{.47}As/In_{.52}Al_{.48}As$ heterosystem, lattice-matched to InP. The emitter layer (*d*) has two contacts, *S* and *D*, and plays the role of a hot-electron cathode. The collector layer (*a*) is separated from the emitter by a potential barrier (*c*). Transistor action consists in the control of the injection current I_C by the voltage V_{DS}, applied between *S* and *D*.



a: 5000 Å InGaAs n^+ (Si:10^{19})
b: 500 Å InGaAs n^- (Si:10^{17})
c: 2000 Å InAlAs u
d 500 Å InGaAs n (Si:10^{16})
e: 25 Å InAlAs n^+ (Si:10^{19})
f: 200 Å InGaAs n^+ (Sn:10^{20})
g: 500 Å Ti / 1000 Å Au
h: Si_3N_4

Fig. 1. Cross-section of a real-space-transfer transistor implemented[4] in the InGaAs/InAlAs heterostructure lattice-matched to InP.
The epitaxially-grown heavily-doped cap layer *f*, forming the *S* and *D* contacts, is lithographically patterned using the etch-stop layer *e*.

The structure shown in Fig. 1 and its variations have been employed in a series of experimental studies.[4,5] Experimental CHINT *IV* characteristics are extremely nonlinear, including a strong negative differential resistance (NDR) in the $I_D(V_D)$ dependence with sharp steps, cf. Fig. 2. Monte Carlo (MC) simulations[6] of the CHINT, demonstrate internal switching and the formation of high-field domains. These instabilities arise due to a positive feedback between the RST and the heating electric field in the emitter channel. Both experimental measurements and MC calculations have been limited in analyzing RST effects due to the restriction of tracing *IV* characteristics exclusively in voltage increments. The present work reviews recent progress in the understanding of the RST instabilities achieved with the help of continuation modeling and transient device simulation.

The study of hot-electron domains in RST transistors is important for understanding device limitations. Switching of the electron-heating control to the collector restricts the range where CHINT can be used as a linear amplifier. The frequency performance of CHINT in its usual mode is believed to be limited only by the time of flight of hot electrons over high-field regions of the device, i.e., over distances of order the barrier-layer thickness. For the device in Fig. 1, the transit time can be estimated to be of order 2-3 ps, which sets the upper limit for unity-gain cutoff frequencies at around 50 GHz. The cutoff frequencies, extrapolated from the microwave measurements of scattering parameters in this structure,[5] were 40 Ghz for both the current and the power gain. The ultimate speed performance can be achieved with an inverted CHINT structure in which the collector is the top layer.[7,8] This allows the reduction of the parasitic drain-collector capacitance and therefore the use of narrower barriers. With sufficiently narrow barriers, the CHINT can be expected to outperform a field-effect transistor of similar geometry (the RST collector corresponding to the FET gate, etc.) because the small-signal performance of CHINT is not limited[1] by the time of flight between the source and the drain. This advantage was recently demonstrated experimentally.[8] However, the domain formation itself seems to be a longer, FET-like, process.

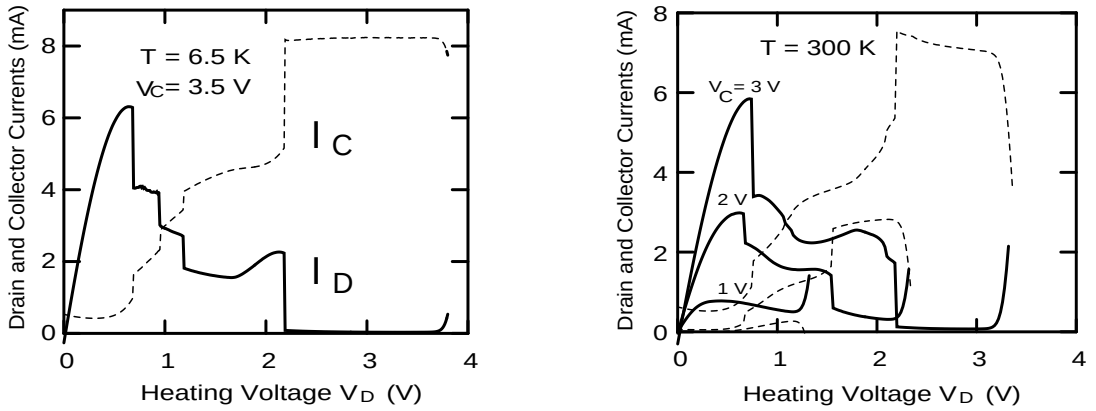


Fig. 2. Experimental InGaAs/InAlAs CHINT *IV* characteristics (a) $T = 6.5$K (b) $T = 300$K. (After Mensz et al.[4])

Perhaps the most interesting potential applications of RST devices are expected to be based on their unique *symmetry property*: the direction of the output (collector) current I_C is the same irrespective of the polarity of the input (heating) voltage V_{DS}. This symmetry, unavailable in other transistors, implies that the output current in CHINT is an exclusive OR function of the input signals $I_C = \mathbf{xor}(V_S, V_D)$. With a load device in the collector circuit, the output voltage is $V_{OUT} = \mathbf{xnor}(V_S, V_D)$. Moreover, we have proposed[9] a new logic device, called the NORAND, that has three symmetric logic inputs $\mathbf{X}_j$ $(j = 1, 2, 3)$ and one output V_{OUT} given by

$$\mathbf{norand}(\{\mathbf{X}_j\}) = (\mathbf{X}_1 \cap \mathbf{X}_2 \cap \mathbf{X}_3) \cup (\bar{\mathbf{X}}_1 \cap \bar{\mathbf{X}}_2 \cap \bar{\mathbf{X}}_3), \qquad (1)$$

where the symbols $\bigcap$, $\bigcup$, and $\overline{\mathbf{A}}$ stand for logic functions **and**, **or**, and **not A**, respectively. The NORAND operates as $\mathbf{nor}(\mathbf{X}_1, \mathbf{X}_2) = \overline{\mathbf{X}_1 \bigcup \mathbf{X}_2}$ when the $\mathbf{X}_3$ input is *low*, $\mathbf{X}_3 =$ logic **0** and as $\mathbf{and}(\mathbf{X}_1, \mathbf{X}_2) = \mathbf{X}_1 \bigcap \mathbf{X}_2$ when $\mathbf{X}_3 =$ logic **1**. The logic functions NOR and AND are interchangeable in the course of a circuit operation. The NORAND function has been demonstrated experimentally.[10]

Similar logic opportunities arise in *optoelectronic* charge injection transistors based on the RST of *minority* carriers into a collector layer of complementary conductivity type.[11] Figure 3 shows the cross-section of such a device recently implemented by Mastrapasqua et al.[12] Its current-voltage and light-voltage characteristics are displayed in Fig. 4. Light output faithfully tracks the RST current and exhibits the $\mathbf{xor}(V_S, V_D)$ function. The internal quantum efficiency η (number of photons emitted per number of electrons injected by RST) depends on the lattice temperature T and the electron injection energy, exceeding 90% at lower T. Efficient light emission has also been demonstrated at room temperature. Moreover, surface emitting lasers have been proposed that function as electrically programmable OR-NAND logic gates with an optical output.[11]

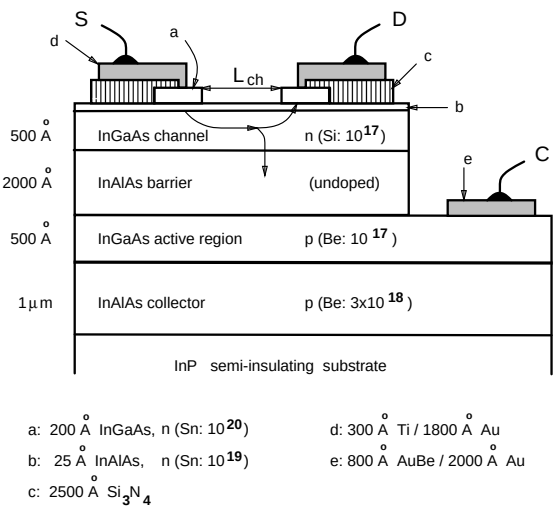


Fig. 3. Cross-section of the complementary-collector charge-injection transistor: a light-emitting RST device (after Mastrapasqua et al.[12])

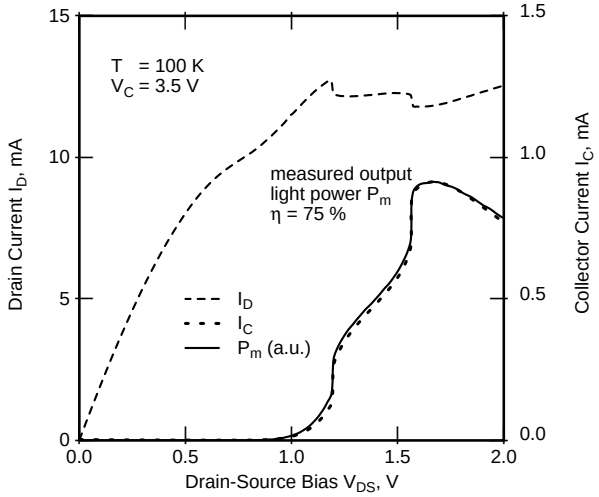


Fig. 4. Current-voltage (solid lines) and optical power-voltage (dashed line) characteristics of the light-emitting RST device. The on/off ratio in P_m exceeds 10^4.

The invention of NORAND has focused our attention on the symmetry properties of RST transistors. The basic CHINT structure is symmetric with respect to reflections in the midplane normal to channel. Hence states of the device at an external bias $[V_D, V_C]$ are related to those at $[-V_D, (V_C - V_D)]$. In particular, states at $V_D = 0$ must either be symmetric or possess broken-symmetry partners. An unexpected recent discovery[13] is the existence of a number of such states, some of which are not only stationary but also *stable* with respect to small perturbations. In these "anomalous" states,[14] the electron heating is due to the fringing field from the collector electrode. Our study shows that the formation of hot-electron domains at $V_D > 0$ represents a transition to a collector-controlled state that is continuously related to one of the anomalous states at $V_D = 0$. Understanding of these processes may stimulate the invention of novel RST devices with an enhanced functionality.

Results of our numerical simulation of the hot-electron transport in a three-terminal RST structure are reviewed below. A number of two-dimensional CHINT simulations have been performed, varying the device geometry (channel length L_{CH} and barrier thickness d_B), transport parameters, and the external bias conditions. Both stationary and time-dependent problems have been investigated.

MATHEMATICAL MODEL

Any model which attempts to account for real-space transfer effects must directly include terms for carrier heating. Further, the ability to specify some form of Neumann boundary conditions is essential for tracing arbitrary, multivalued *IV* characteristics. Both of these requirements are met by the general-purpose device simulator PADRE[15] which solves partial differential equations derived from moments of the Boltzmann equation. In the following, we have used the energy balance system[16, 17], defined in terms of the electrostatic potential ψ, the electron density n, and the electron temperature T_e as follows:

$$\nabla\cdot(\varepsilon\nabla\psi) = -q(p-n+N) \tag{2}$$

$$\frac{\partial(qn)}{\partial t} = \nabla\cdot\mathbf{J} \tag{3}$$

$$\nabla\cdot\mathbf{S} = \mathbf{J}\cdot\mathbf{F} - \frac{3n}{2}\frac{k(T_e-T)}{\tau_e} - \frac{3}{2}\frac{\partial(nkT_e)}{\partial t}\,. \tag{4}$$

The electron current density **J** and energy flux **S** are given by

$$\mathbf{J} = q\mu n\mathbf{F} + \mu\nabla(nkT_e) \tag{5}$$

$$\mathbf{S} = -\frac{5}{2}\frac{kT_e}{q}\left[\mathbf{J} + \kappa_0\mu n\nabla kT_e\right]. \tag{6}$$

In Eqs. (2) − (6), q is the electronic charge, p is the hole density (a function of ψ), k is Boltzmann's constant, ε is the permittivity, μ is the mobility, τ_e is the energy relaxation time, κ_0 is a dimensionless heat conduction coefficient, and **F** is the carrier driving force, including quasi-fields (i.e., from local band-gap variations).

Through an element-based data structure, PADRE decomposes a device domain into arbitrary, nonplanar configurations of regions; for instance, any number of heterointerfaces can terminate abruptly at a single location (node). Data at the verticies of each element can have local material and model dependencies, e.g. μ, ε, τ_e, and k_0 in Eqs. (2)-(6). The impurity concentration N and solution variables are allowed to change abruptly across any heterostructure interface. In this analysis, the quasi-Fermi level and T_e are assumed continuous, thus introducing a T_e dependence in the interface condition on local electron density n; for Boltzmann statistics, this condition reduces to

$$\frac{n^{(m2)}}{n^{(m1)}} = \frac{N_C^{(m2)}}{N_C^{(m1)}}\exp\left[-\frac{\Delta E_C(m2-m1)}{kT_e}\right] \tag{7}$$

at an interface between materials $m1$ and $m2$, where ΔE_C is the conduction band offset and N_C represents the density of states. These relations imply that the RST current density at energy barriers is thermionic and included self-consistently.

Models for μ and τ_e as a function of T_e are typically derived from user-defined (e.g. MC) velocity-field $v(F)$ and temperature-field $T_e(F)$ relations for homogeneous slabs. To avoid confusion with negative differential mobility effects arising from momentum space transfer, a single population of electrons has been used here with a monotonic $v(F)=\mu_0 F[1+(\mu_0 F/v_{sat})^2]^{-1/2}$ relation[18] together with the $T_e(F)$ implied by a T_e-independent diffusivity[19] and a consistent[16] κ_0. We have checked that our results remain qualitatively similar for more realistic $v(F)$, $T_e(F)$. For similar reasons, impact ionization and tunneling effects were excluded. Other parameters were selected to match the InGaAs/InAlAs system as exactly as possible. Of critical importance is the barrier height, taken as $\Delta E_C = 0.5\,\text{eV}$; the low field mobility μ_0 was assumed a function of the local ionized impurity concentration such that $\mu_0 \approx 10^4\ \text{cm}^2/\text{V}\cdot\text{sec}$ in the emitter.

In order to trace the complex *IV* curves shown below, it is necessary to apply mixed current/voltage boundary conditions. We have used predictor-corrector continuation[20] based on a pseudo-arclength σ for this purpose. Computationally, the continuation method requires the addition of a single algebraic auxiliary equation, typically written in terms of the voltage and current (V_j, I_j) and the unit tangent $(\dot{V}_j, \dot{I}_j)$ at a known point on the curve j.

The unit tangent can also be used to detect limit points (e.g. where $\dot{V}=0$ or $\dot{I}=0$) and to predict an initial guess for the subsequent bias point j+1. Fig. 5 illustrates the continuation method and associated auxiliary condition on the pseudo-arclength used here.

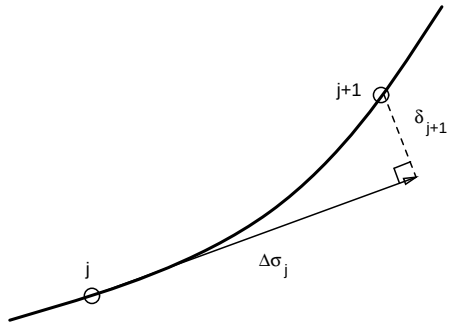


Fig. 5: Predictor-corrector continuation applied to step between consecutive points j and j+1 on an *IV* curve. The corresponding auxiliary equation is

$$\dot{I}_j\,(I-I_j)+\dot{V}_j\,(V-V_j)-\Delta\sigma_j \;=\; 0$$

where the next pseudo-arclength step $\Delta\sigma_{j+1}$ is automatically controlled by a user-specified tolerance on the error of the tangential projection δ_j.

BROKEN SYMMETRY AND FORMATION OF RST DOMAINS

Rapid Ramping. Figure 6 illustrates a time-dependent simulation of a device with $L_{CH}=5\,\mu$m and $d_B=0.2\,\mu$m. Both *S* and *D* electrodes are kept grounded, while V_C is linearly ramped from 0 to $V_C=2$ V. Depending on the ramping time τ the device settles in one of two states: for $\tau>\tau_{cr}$ it is the normal[14] state, whereas for $\tau<\tau_{cr}$ the steady state carries a large RST current (Fig. 6a). The critical ramping speed is determined by the rate at which the increasing fringing field (Fig. 6b) is screened by channel electrons. The value of $\tau_{cr}\approx 32.3$ ps roughly corresponds to the time of electron travel from *S* and *D* contacts to the middle of the channel.

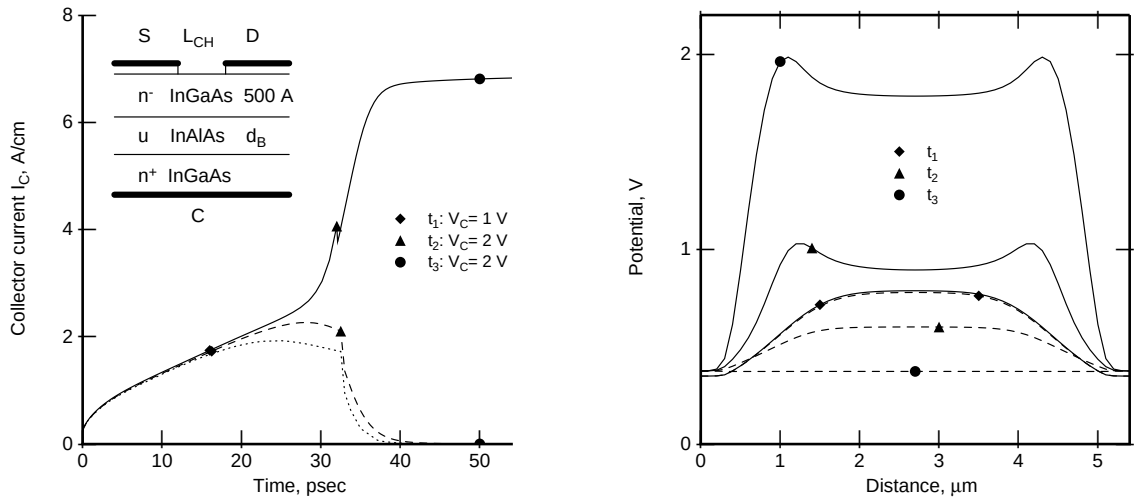


Fig. 6. Time-dependent simulation of a real-space transfer transistor with $L_{CH}=5\,\mu$m, $d_B=0.2\,\mu$m, and $v_{sat}=10^7$ cm/s. The collector voltage is ramped linearly from $V_C=0$ at $t=0$ to $V=2$ V at $t=\tau$. The results are plotted for two situations: $\tau=32.0$ ps $<\tau_{cr}$ (solid lines) and $\tau=32.5$ ps $>\tau_{cr}$ (dashed lines).
(a) *left figure*: Collector current $I_C(t)$; inset shows cross-section of the device structure. Dotted curve corresponds to the absence of a RST (pure displacement current); it is obtained by artificially increasing the barrier height.
(b) *right figure*: Potential distribution $V(x)$ along the channel at selected times.

The anomalous state at $V_D = 0$ exists only for a sufficiently high V_C, and the value of V_C^{cr}, below which this state disappears, depends on the device geometry and v_{sat}. The value of V_C^{cr} is sharply defined, and for the ramp end voltage V above V_C^{cr}, one has $\tau_{cr} \propto V$ to a good approximation, cf. Fig. 7a. This indicates that the relevant critical parameter is the displacement current ($\propto dV/dt$), which should be compared to a transient current ($\propto v_{sat}$)

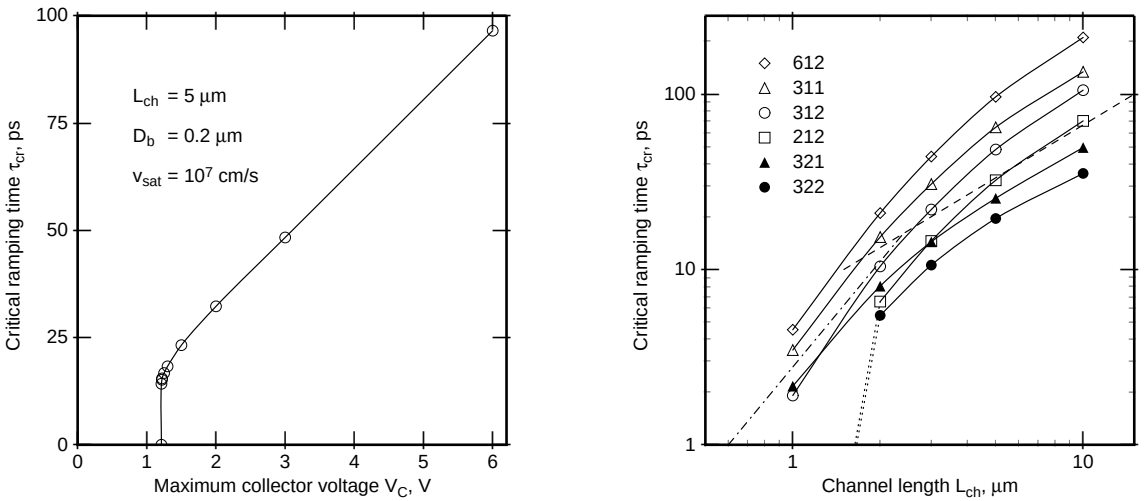


Fig. 7. Critical ramping speed for the formation of a stable anomalous stable state at $V_D = 0$. The collector bias is ramped linearly $V_C = 0 \to V$ in the time interval τ. For $\tau > \tau_{cr}$ the device settles in the normal state, for $\tau < \tau_{cr}$ in the anomalous state (in the notation of Fig. 8 this is state **d**).
(a), *left figure*: The dependence of τ_{cr} on the endramp voltage for a 5 μm device. For this device $V_C^{cr} = 1.21$ V.
(b), *right figure*: The curve labels *VSD* indicate the endramp voltage (V) in volts, the saturated velocity (S) in 10^7 cm/s and the barrier thickness (D) in 1000 Å. The dashed and stipple lines indicate linear and quadratic dependences, respectively.

associated with electron screening processes in the emitter. The values of τ_{cr}, determined to within 0.1 ps, are plotted in Fig. 7b against the emitter channel length L_{CH} for different assumed values of v_{sat}, barrier thicknesses, and ramp end voltages V. For short L_{CH} the dependence $\tau_{cr}(L_{CH})$ is approximately quadratic, and for long L_{CH} the dependence is linear.

Stationary Characteristics. Starting from the two stationary states at $V_D = 0$, we were able to determine the characteristics $I_D(V_D)$ and $I_C(V_D)$ at a fixed collector voltage $V_C = 2$ V relative to the S electrode. With the predictor-corrector continuation method[20], we can trace arbitrarily shaped, connected components of the characteristic, starting from any established state within each component. The curves in Fig. 8 correspond to the locus of points in the (V_D, I_D) plane for which the device has a steady state at a given V_C. To our knowledge, the displayed $I_D(V_D)$ dependence represents the first example of a multiply connected current-voltage characteristic. Any transition between disconnected components of the graph requires a global redistribution of the state fields corresponding to the formation or repositioning of high-field, high-temperature domains in the structure. Such a redistribution, reminiscent of a phase transition, is forced as V_D increases beyond the rightmost point (**k**) of the bounded graph component.

The potential profiles $V(x)$ along the channel − before and after the transition − are shown in Fig. 9. Of the three collector-controlled states, **s**, **t**, and **u**, corresponding to the same ($V_D \approx 0.82$ V) external bias as the state **k**, two (**s** and **u**) are stable. The actual transition occurs into the state **u** which has the highest value of the collector current. This has been ascertained by a time-dependent simulation in which the initial state **k** was perturbed by a small step $V_D(\mathbf{k}) \to V_D(\mathbf{k}) + \delta V_D$. The hot-electron domains in the state **u** are characterized by a strong field concentration, accompanied by a dramatic rise in T_e. The electron concentration in the domain is depleted so that

the collector field remains unscreened and the local potential goes below that of the drain, resulting in a negative I_D. All states on the **p** – **u** – **d** branch of the collector-controlled component are similar to **u** and perfectly stable.

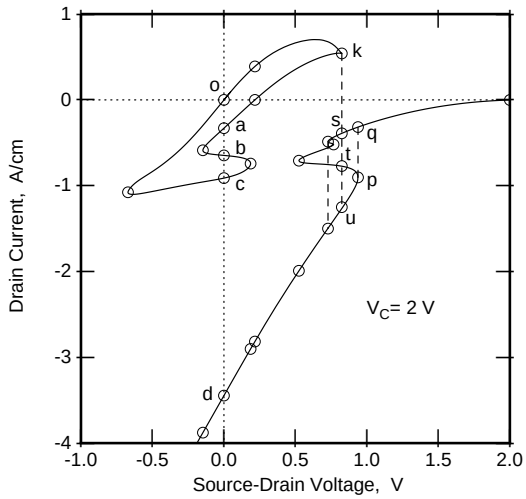


Fig. 8. Current-voltage characteristics obtained by the continuation method.

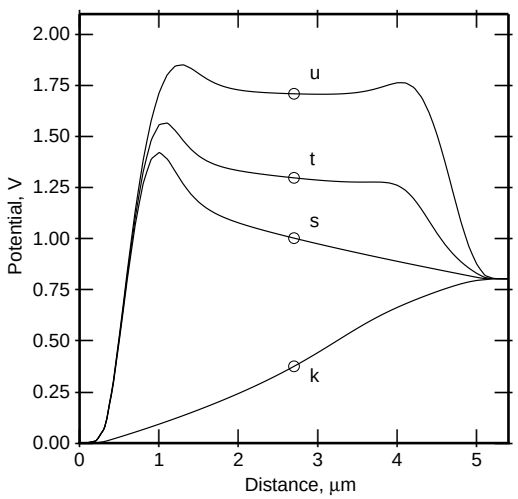


Fig. 9. The channel potential profile $V(x)$ in different CHINT states at the same external bias ($V_C = 2\,\text{V}$, $V_D = 0.825\,\text{V}$).

This indicates that state **d** (which we had first found in rapid ramping of V_C at $V_D = 0$, cf. Fig. 6) is experimentally accessible by a quasi-static variation of V_D at fixed V_C. The existence of a stable anomalous state **d** is obviously a necessary (though insufficient) condition for the multiply-connected topology of the $I_D(V_D)$ characteristic. As discussed above, it results when the competition between RST and screening of the fringing collector field is resolved in favor of RST. Precisely when this happens depends on the transport parameters assumed and the device geometry.

Unstable anomalous states. In addition to the normal state **o** and the anomalous state **d**, Fig. 8 reveals three other anomalous states (**a**, **b**, and **c**) at $V_D = 0$. The profiles $V(x)$ along the channel in these states are shown in Fig. 10.

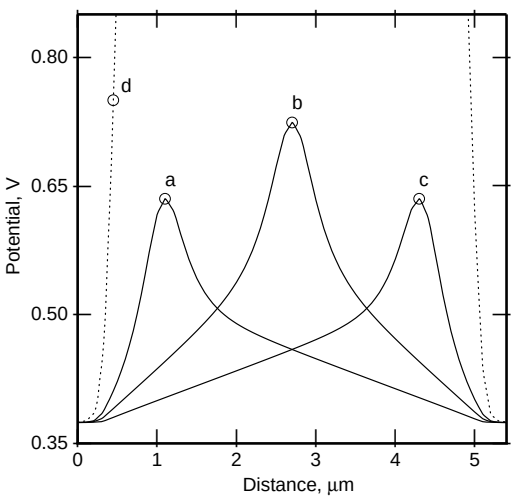


Fig. 10. The channel potential in the four anomalous states at $V_D = 0$.

It is clear that because of the non-linear nature of the problem, the actual stationary states may not transform according to irreducible representations of the symmetry group of the equations governing the device behavior at $V_D = 0$. The distribution of internal fields in the anomalous states is either fully symmetric or these states form a set of partners and transform into one another under the symmetry operations. Thus, states **a** and **c** under reflection transform into each other, even though the group has only one-dimensional linear representations. On the other hand, states **o**, **b**, and **d** are symmetric. Biasing the *D* electrode with respect to *S* breaks the reflection symmetry and allows a continuous transformation between states of different symmetry on the loop.

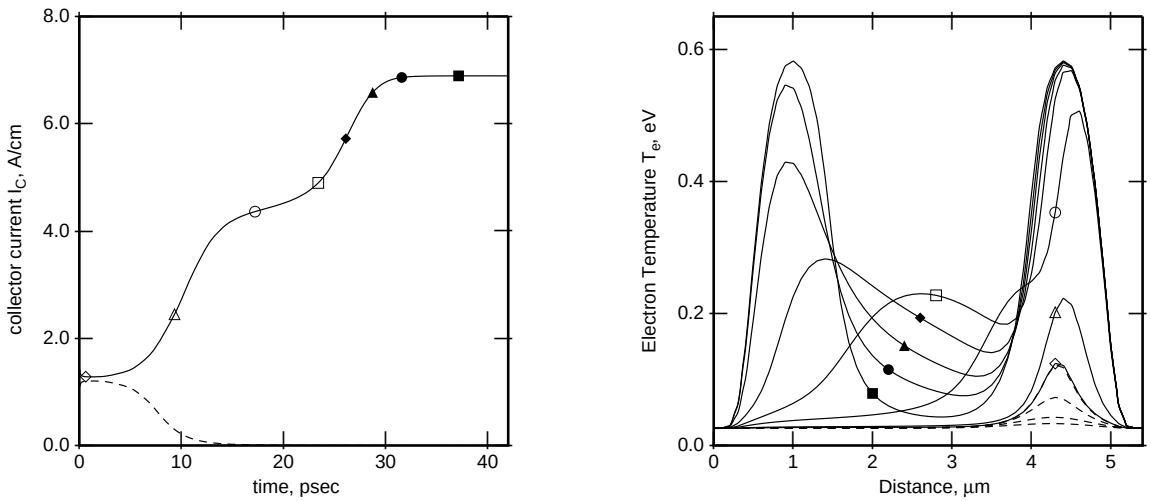


Fig. 11. Evolution of the non-stationary states $\mathbf{c}_+$ (solid lines) and $\mathbf{c}_-$ (dashed lines) at $V_D = 0$. Time dependence of the injection current is shown in *the left figure*; symbols mark the selected times in the evolution, at which the electron temperature profiles are plotted in *the right figure*. The "plateau" in the $I_C(t)$ dependence near $t = 20$ ps evidently corresponds to the situation when a fully-developed hot-electron domain exists already near *D* but not yet near the *S* electrode.

Of the five states at $V_D = 0$ and $V_C = 2$ V, only two (**o** and **d**) are stable with respect to small perturbations. This has been ascertained by following the evolution of states in the vicinity of the steady states at $V_D = 0$. In these simulations, Fig. 11, the initial states $\mathbf{a}_\pm$, $\mathbf{b}_\pm$, and $\mathbf{c}_\pm$ have been assumed to coincide with a state on the loop displaced from **a**, **b**, and **c**, respectively, by an infinitesimal voltage $\delta V_D = \pm 10$ mV. Even though these states are virtually indistinguishable from the corresponding stationary ones, we found that $\mathbf{a}_+$, $\mathbf{b}_-$, and $\mathbf{c}_-$ evolved into **o**, while $\mathbf{a}_-$, $\mathbf{b}_+$, and $\mathbf{c}_+$ into **d**. All these instabilities develop on a rapid time scale, corresponding to the electron travel over the distances of the order of the domain size. They result in either the formation (repositioning) of a hot-electron domain, or its complete quench due to the screening by channel electrons.

Note that the question of stability of a given state can usually be ascertained *without* costly time-dependent simulations − by inspecting the phase diagrams $I_D(V_C, V_D)$ and $I_C(V_C, V_D)$ discussed below. The instability of states **a** and **c** is associated with a NDR in the $I_C(V_C)$ dependence, $\partial I_C/\partial V_C < 0$, and that of **b** with both $\partial I_C/\partial V_C < 0$ and $\partial I_D/\partial V_D < 0$. No counterexample to this rule has yet been found.

DC mappings of CHINT current-voltage characteristics. Fig. 12 shows $I_D(V_{DS})$ characteristics for a single device at $T = 300\,\mathrm{K}$ using a series of fixed collector voltages (V_{CS}). Close examination of the characteristics shows numerous topological transformations. Beginning as an accumulation mode FET at low V_{CS} ($<1.0\mathrm{V}$), the onset of RST initiates the formation of a slight NDR region in the $+V_{DS}$ direction ($\simeq 1.0\mathrm{V}$). At higher V_{CS}, separate folds begin to appear for both $V_{DS} > 0$ and $V_{DS} < 0$, although the curves remain singly connected. At $V_{CS} \simeq 1.2\mathrm{V}$, a disconnected loop begins to appear in the left-hand plane, corresponding to a surface bounded by a minimum V_{CS} in the 3D space in Fig. 12. As shown in Fig. 13 ($V_{CS} = 1.5\,\mathrm{V}$), this closed loop and the needle-like fold emanating from the bottom of the left-hand plane both continue to open, and the ''S-shaped'' notch in the right-hand plane (the knee reached by tracing backwards from $V_{DS} = +\infty$) moves leftward as V_{CS} increases. By $V_{CS} = 1.6\,\mathrm{V}$, the characteristic is transformed into a loop which includes the origin, and a singly connected component which is multivalued but has no folds or intersections with the loop. These two components maintain essentially the same topology for larger V_{CS} although their separation in (I,V) increases, cf. Fig. 8.

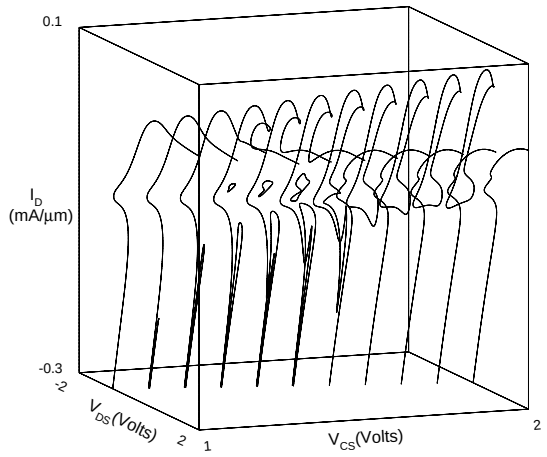


Fig. 12: CHINT I_D-V_{DS} characteristics for $1.0\mathrm{V} \le V_{CS} \le 2.0\mathrm{V}$ ($L_{CH} = 5\mu\mathrm{m}$, $d_B = 0.2\mu\mathrm{m}$, $v_{sat} = 1\times10^7\,\mathrm{cm/s}$). Curves represent simulations at constant V_{CS} separated by $\Delta V_{CS} = 0.1\mathrm{V}$.

Note the multiplicity of anomalous $V_{DS} = 0$ states. In general, at $V_{DS} = 0$, we can expect an odd number m_S of symmetric states and an even number m_A of asymmetric ones, because there should always be one and only one unbounded path in the (V_{DS}, I_D) plane, while, by symmetry, asymmetric states come in pairs. Varying V_{CS}, we have been able to realize cases with $(m_S, m_A) = (1,0)$, $(3,0)$, $(3,2)$, $(3,4)$, and $(5,4)$. In a continuous variation of V_{CS} one can, of course, arrive at a situation when the $I_D(V_{DS})$ curve only touches the $V_{DS} = 0$ axis without crossing. At this singular point there is an accidental degeneracy of two symmetric states, and the total number of distinct symmetric states becomes even.

Interestingly the symmetry partners may belong to topologically disconnected branches of the I_D–V_{DS} characteristic. It is in fact the existence of unpaired asymmetric states along the singly connected, outer curve in Fig. 13 that has led us to the discovery of the loop, disconnected from the origin.

Figure 14 shows a map of the I_C-V_{DS}, corresponding to the I_D-V_{DS} plot in Figs. 13. Together, they completely define the device state since $I_C = I_S + I_D$. Although slices of I_C-V_{DS} space for a given V_{CS} are not symmetric, there is symmetry in the 3D space defined by $I_C(-V_{DS},\, V_{CS} - V_{DS}) = I_C(V_{DS},\, V_{CS})$. Since the collector current is invariant under the symmetry transformation, plots of I_C-V_{DS} have many self-intersections, cf. Fig. 14. Points defined by a single intersection with the $V_{DS} = 0$ axis correspond to symmetric states ($I_C = 2I_D = 2I_S$); points defined by two coincident intersections represent reflective, asymmetric pairs.

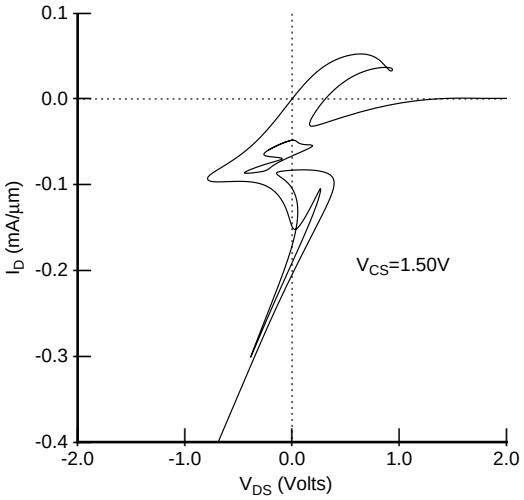


Fig. 13: Single CHINT I_D-V_{DS} characteristic from Fig. 12 for V_{CS} = 1.50 V which contains both a self-intersecting component and a disconnected loop.

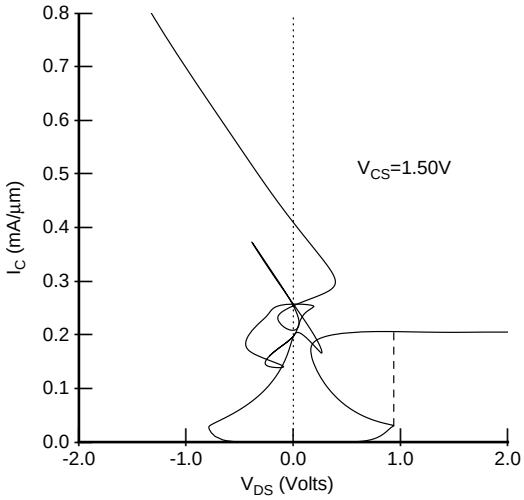


Fig. 14: Single CHINT I_C-V_{DS} characteristic for V_{CS} = 1.50 V corresponding to the I_D-V_{DS} in Fig. 13.

Phase space mappings, like those represented by curves in Figs. 13 and 14, have the property that except in the vicinity of self-intersections, their infinitesimally close points correspond to infinitesimally close state vectors $\mathbf{z} \in \boldsymbol{R}$ in the multidimensional space $\boldsymbol{R}$, describing the state of the device [i.e. all the fields $n(x,y)$, $T_e(x,y)$, $\psi(x,y)$, etc.]. The converse is always true: points separated by a finite distance on a (V, I) plane correspond to macroscopically distinct states **z**. Continuation in the pseudo-arclength produces a completely smooth evolution of the device state. In contrast, experimental measurements (and MC simulations) force abrupt transitions at limit points, for instance **k**→**u** in Figs. 8, as V_{DS} is increased from 0, corresponding to the formation or repositioning of a high-field, high-temperature domain. The resultant negative I_D at **u** arises as the potential in the hot electron domain is lower than that of the drain, due to the unscreened collector field.

Fig. 15 shows the results of continuation simulations started from the origin for $V_{DS} > 0$, using a higher saturation velocity v_{sat}. Both the V_{CS} and V_{DS} thresholds for causing folds or limit points in IV increase with v_{sat}. The thresholds are reduced for smaller L_{CH}, see Fig. 16. These dependencies are similar to those described above in connection with the critical ramp speed of a transient V_{CS} excitation required to induce the stable **d** state at V_{DS} = 0.

In spite of the somewhat artificial $v(F)$ and $T_e(F)$ assumed for our present purposes, we believe it can be safely concluded that the cause of the nonlinear steps observed past the RST threshold in experiments are the loops and folds predicted by continuation. Transient simulations corresponding to measurement procedures indicate that folds (e.g. in Fig. 15 for V_{CS} = 3.0 V) can be followed to some length. Predictions of where the state transition will occur can be extracted accurately from complete dc IV maps, but this analysis must include consideration of NDR effects at all terminals as well as external circuit configurations.

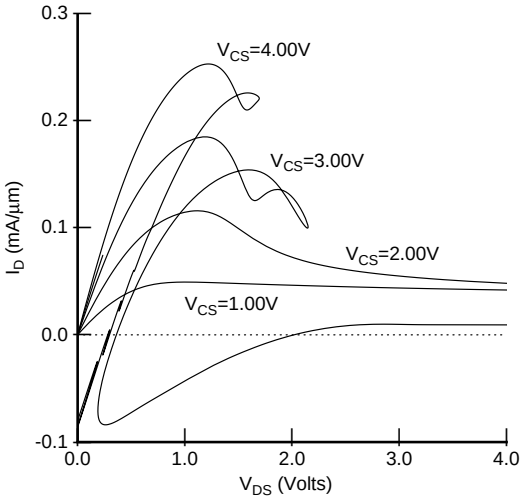


Fig. 15: CHINT I_D-V_{DS} characteristics as a function of V_{CS} ($L_{CH} = 5\,\mu m$, $d_B = 0.2\,\mu m$, $v_{sat} = 2\times10^7\,cm/s$). Results are shown only for the $V_{DS} > 0$ branches initiated from the origin.

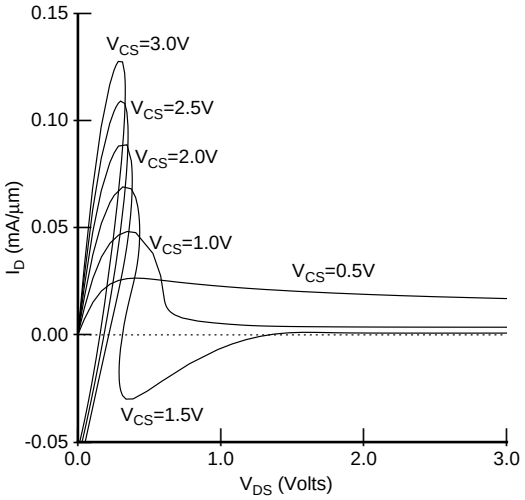


Fig. 16: CHINT I_D-V_{DS} characteristics as a function of V_{CS} ($L_{CH} = 2\,\mu m$, $d_B = 0.2\,\mu m$, $v_{sat} = 1\times10^7\,cm/s$). Results are shown only for the $V_{DS} > 0$ branches initiated from the origin.

CONCLUSION

We have found that charge injection transistors possess complicated − often multiply-connected − *IV* characteristics. Application of a sufficiently high V_{DS} at a fixed $V_{CS} > 0$ forces a switching transition, accompanied by the formation of a hot electron domain. Physically, the domains form when the finite supply rate of electrons to a "hot spot" is exceeded by the RST flux from that spot. The depleted domains unscreen the fringing field ("normally" screened by channel electrons) and the RST becomes collector controlled.

Potential applications of RST devices are likely to be based on their peculiar symmetry with respect to the heating field polarity. The same symmetry shows up in the analysis of the hot-electron domain formation. States of a multiterminal RST device under general bias are "adiabatically" connected to the anomalous states of the symmetric configuration at $V_D = 0$. The symmetry analysis is likely to prove very potent with devices of more complicated geometry, such as the NORAND, whose symmetry group is C_{3v}. We believe the phenomena that occur at $V_{DS} = 0$ capture the essential physics associated with the RST domains in general.

Our results were obtained using a transport model which eliminates the usual instabilities resulting from a negative differential mobility (the latter has been artificially excluded). We have verified that all our observations remain qualitatively valid with a more realistic velocity-field model appropriate for InGaAs. For a quantitative simulation of a particular RST device structure one would clearly need a realistic transport model; we would like to stress, however, that the novel anomalies discussed in this work can be qualitatively reproduced in *any* model that allows channel electrons to be heated and self-consistently includes the RST flux.

An essential feature of our analysis is the use of continuation methods which allow the inspection of the full device phase space. Slicing the $I_D(V_D, V_C)$ surface at different V_C, we find $I_D(V_D)$ curves of different topologies. The internal fields evolve smoothly along a connected $I_D(V_D)$ trajectory and do not signal the approach of a switching transition. Phase-space mappings successfully give the global type of information. Moreover, they usually give an unerring guess as to the *stability* of a given state, subsequently supported by costlier transient simulations. The understanding gained in this fashion will be invaluable in the application of RST transistors to the design of high-performance systems.

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